Commercialization of High 600V GaN-on-Silicon Power Devices

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Abstract. With power conversion losses endemic in all areas of electricity consumption, broadly categorized into motion control (accounting for around 50% of total electrical energy use), lighting, air conditioning, and information technology, consumers, governments and utilities are finding ways to achieve higher efficiency. Manufacturers of data servers, telecom systems, solar power inverters and drives for motor control are focused on reducing power conversion losses while simultaneously shrinking the size of power systems. Although silicon has historically been the base device material used by the power conversion industry, it is rapidly reaching its physical performance limits. GaN semiconductors solutions reduce power conversion loss by over 50% in a significantly smaller form factor and at a lower cost, when device design, fabrication technology and application design are holistically combined to deliver superior end products.

1. Introduction

With no luxury of profiting from early low-performing devices and slowly improving upon them, GaN power product developers have a short runway to completely understand technical issues and effectively and reliably execute engineering tasks for the 1st product to surpass performance of the established Si completion. Applications also need to be identified where the overall benefit is sufficient to amortize the inevitably higher initial device cost. Following the technological and commercial success of GaN based LED and microwave products [1,2], the commercialization of GaN-based transistors and diodes for power conversion is now a reality. First-generation 600-V class EZ GaN™ HEMTs and diodes were successfully produced at Transphorm Inc. with the aforementioned considerations. The low on-resistance, low capacitance and high switching frequency for GaN devices enables high conversion efficiency, hence energy savings, in a compact form factor.

2. GaN Device and Module Architectures and Examples of End Benefit

The GaN HEMT switch incorporates a normally-off low-voltage Si device at the input and a normally-on high-voltage GaN HEMT at the output in a cascode configuration. The hybrid device has +2.1V gate threshold and maximum gate swings of ±18V, easily driven by low-cost MOSFET gate drivers. The on-resistance ranges from 250 to 150 mΩ based on device size. Comparing to similarly-rated state-of-the-art Si super-junction MOSFETs on the market, the GaN devices offer significant reduction in gate charge, on-resistance and output capacitance. The finished device in a TO-220 package also features the Quiet-Tab™ package scheme, with Gate-Source-Drain (GSD) pin-out arrangement and the package base as a low-inductance source terminal. This configuration allows 200% increase in switching speed compared to traditional TO-220 packages, which is necessary to take full advantage of the low switching losses of GaN. The GaN diode has a Schottky barrier with a forward voltage of 1.3V at 4-8 A current depending on size, with no minority or reverse recovery charges.
Two key application examples are discussed next. A 750-W, 230-400V boost converter with the total-GaN solution (using both GaN HEMT & GaN diode) was designed which showed cleaner and faster waveforms as well as 33% and 70% reductions of device losses at 100 and 500 kHz respectively compared to a converter with the state-of-the-art Si transistor and Si diode in the market. The hybrid GaN HEMT is also capable of three-quadrant operations and has 25-time less reverse recovery charge than the best Si super-junction MOSFETs. This makes diode-free hard-switched bridge possible. 600-V 6-in-1 power modules with on-resistance of 150 mΩ per switch were developed for operation at 100-300 kHz, about 10-times higher than traditional power modules. The high PWM frequency allows integration of compact output filters resulting in a 3-phase pure-sine-wave inverter for PV or motor drive application. An actual motor operation test at 100-kHz PWM has revealed significant electro-mechanical efficiency boost by the GaN inverter by 8%, 4% and 2% at low, mid and high load respectively, compared to a state-of-the-art IGBT inverter at 16 kHz [3].

3. Device Manufacturing and Performance

GaN epi-layers were grown on 4”-6” SiC and Si substrates. These epi films were developed to have a low defect density, high 2-DEG mobility and high charge density such that both a high breakdown field and a low channel resistance are achieved. Depletion mode GaN-based HEMTs were then manufactured in fabrication facilities including lithography, etching, CVD deposition, metallization, and other requisite steps.

Figure 3. GaN/Si and GaN/SiC HEMT leakage comparison data shows minimal impact of dislocations/GaN-Si material on achieving comparable and lower leakage than GaN on SiC devices.
The finished wafers are characterized with auto probers of high current and high voltage capabilities. The typical on-wafer off-state drain leakage $I_D$ and gate leakage $I_G$ of 120-mm-wide HEMTs are shown in fig.1. At $V_D=600V$, the room temperature drain leakage is as low as 10-50nA and gate leakage is 3-15nA. At 150C, the typical drain leakage increased to 1-10μA and gate leakage is about 0.1-1μA at 600V. Contrary to the popular myth, dislocations do not impact the leakage current levels in otherwise well designed and optimally manufactured lateral GaN devices, as evidenced by the similar leakage performance of our GaN on Silicon HEMTs compared to our GaN on SiC HEMTs (Figure 3).

The typical DC on-resistance of 120mm GaN HEMT is about 0.12 Ω and the capacitance ($C_{oc}$) is 56 pf. As any well designed device should incorporate, and is evident from the leakage currents, our 600V rated devices have breakdown voltages in excess of 900V. We have also tested the robustness of these devices against spikes, by intentionally subjecting them to up to 900V spikes (1Million spikes) in a true switching environment. No performance degradation is observed. In production, 100% spike testing is performed to 750 volts (figure 4). While the present breakdown voltage is much lower than the inherent avalanche capability of GaN material, the design margin available in our devices guarantees against failure in appropriately designed end user circuits and applications.

Good dispersion control is the key to achieve the low on-resistance in switching operation. Small devices were used for on-wafer evaluation of dynamic performance. The increase of dynamic Ron from static to 500V is usually around 20% or less. The dynamic performance is again verified in final packaged devices, guaranteeing that users of this device will indeed match up-in-circuit performance with datasheet values of resistance- a key feature lacking from typical GaN devices that have surfaced on the market in past. The dynamic Ron of packaged device measured with low duty cycle at various pre-bias voltages is shown in figure 5. It increased only 0.01Ω from 0 to 200V and then saturated up to 600V.

![Previous status: Mid 2008](image1)

![Previous status: End 2008](image2)

![2009](image3)

*Figure 5. Dynamic on-resistance for GaN HEMTs. It is important to achieve no increase in on-resistance at AC conditions to realize high performance in applications.*

High uniformity and repeatability across the wafer and across wafer lots is required to deliver high volume production. Through systematic development, this has been improved by the optimized processing and epitaxial growth. The percent standard deviations of drain leakage and gate leakage at 600V are about 5-10% within one 4” wafer, shown in Figure 6. For DC $R_{on}$, the percent standard deviation is less than 1%. Similarly, good process capabilities ($C_p$ and $C_{pk}$) have been realized on our production platform. Citing the GaN diode as an example, $C_{pk}$ of over 1.2 have been achieved for $V_f$ and $I_r$, two of the most critical end parameters (Figure 7). Behind this is the full capability of individual process step / unit step parameters in our fabrication line.
3. Normally Off GaN HEMTs

Normally off GaN transistors incorporate a cascode approach at the packaged level. As shown in Figure 8, a normally-off low-voltage Si FET was connected to normally-on high-voltage GaN HEMT in series while the gate of the GaN HEMT was connected to the source of the Si FET. This hybrid configuration produced an effective e-mode power device, safe in case of faulty gate control. Moreover, it provides the compatibility with existing Si drivers, as well as the freedom to optimize of GaN HEMTs without complication for input circuits. The plastic-packaged GaN HEMT has a gate threshold of +2.1V typical at 1mA drain current and the drain leakage is 10 μA typical at \( V_G=0\)V and \( V_D=600\)V at 150 °C. The dynamic on-resistance is 0.15 Ω typical. The pulsed drain current is 70 A at a \( V_G=8\)V and \( V_D=10\)V. The continuous (CW) drain current is 14A at a case temperature of 25 °C. Compared with similarly-rated state-of-the-art Si super-junction MOSFETs on the market, this 1st generation GaN HEMT has a better performance in lower on-resistance, higher pulsed current capability and reduced output charge. \( R_{on} \cdot Q_g = 1\)ns and \( R_{on} \cdot Q_{tr} = 8.5\)ns, a significant enhancement already over the mature Superjunction MOSFET technology.

4. 600V GaN on Silicon Qualification

Our team has completed the first qualification of 600V GaN on Silicon devices earlier this year, dispelling the doubt that high voltage GaN can ever be qualified. The qualification testing followed JEDEC standards and comprised of:

1) Accelerated stress and reliability testing on 3 lots of 77 parts each, per JESD-47 standard specification. The requirement to pass is 0 fails across the lots, as per Figure 9. Specific testing included:
i) HTRB: Tj=150ºC, 480V, min: 1000 hrs.

ii) HAST: 130ºC/85% RH, 33.3 psi, continuous bias @100V, min: 96 hrs.

iii) Temperature Cycle: -55ºC / 150ºC, 2 cycles per hour, min: 1000 cycles

iv) Power Cycle: 25ºC / 150ºC, AT = 125ºC, min: 5000 cycles

v) HTSL: 150ºC, min: 1000 hrs.

2) Electrostatic Discharge Tests (Charged Device Model, Machine Model & Human Body Model)

3) Mechanical testing including destructive physical analysis, wire pull, ball shear and die shear, vibration, shock and visual verification.

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All before-after test parameters were measured to confirm adherence to standards to pass qualification testing. As an example, the logarithmic values of mean and standard deviations of high voltage 600Volt GaN HEMT leakage before and after stress testing is shown in Figure 10. To get further confidence for longer term operation, we completed 2000 hours high temperature operating life (HTOL) data on GaN HEMTs running in actual boost power converters at 300 KHz providing 1:2 (200V to 400V DC) boost operation. The junction temperature was 175 ºC. A Silicon reference device was also run to track system variations (e.g. ambient temperature drifts). No degradation of performance during the 2000 hour operation was observed (Figure 11), and all key parameters tested before-after the HTOL life test showed no discernable change.

5. Summary

Development of high-quality GaN epi and GaN device manufacturing technology has generated viable 600-V class GaN products. These devices not only have excellent DC and dynamic characteristics but proved to be superior in actual electricity power conversion application. Our team
has completed the qualification of 600V GaN, an industry first, which allows our customers-partners to now introduce energy saving power conversion products with the performance-cost benefits of GaN on Silicon. These first generation GaN power devices are just the beginning of a long journey for GaN in redefining power conversion for a more energy efficient world.

References