

## Application Note:

### TDPS2800E2C1 Totem Pole PFC Evaluation Board

#### 1. Introduction

The Evaluation Board for a bridgeless totem-pole Power-Factor-Correction (PFC) circuit, using Transphorm GaN power HEMTs, is described in this paper. In this board, by using a diode-free GaN power HEMT bridge with low reverse-recovery charge, very-high-efficiency single-phase AC-DC conversion is realized. In this circuit, the performance and efficiency improvement, achieved by use of the GaN HEMTs in the fast-switching leg of the circuit, is further enhanced by use of low resistance MOSFETs in the slow-switching leg. The evaluation board is shown in Fig. 1.

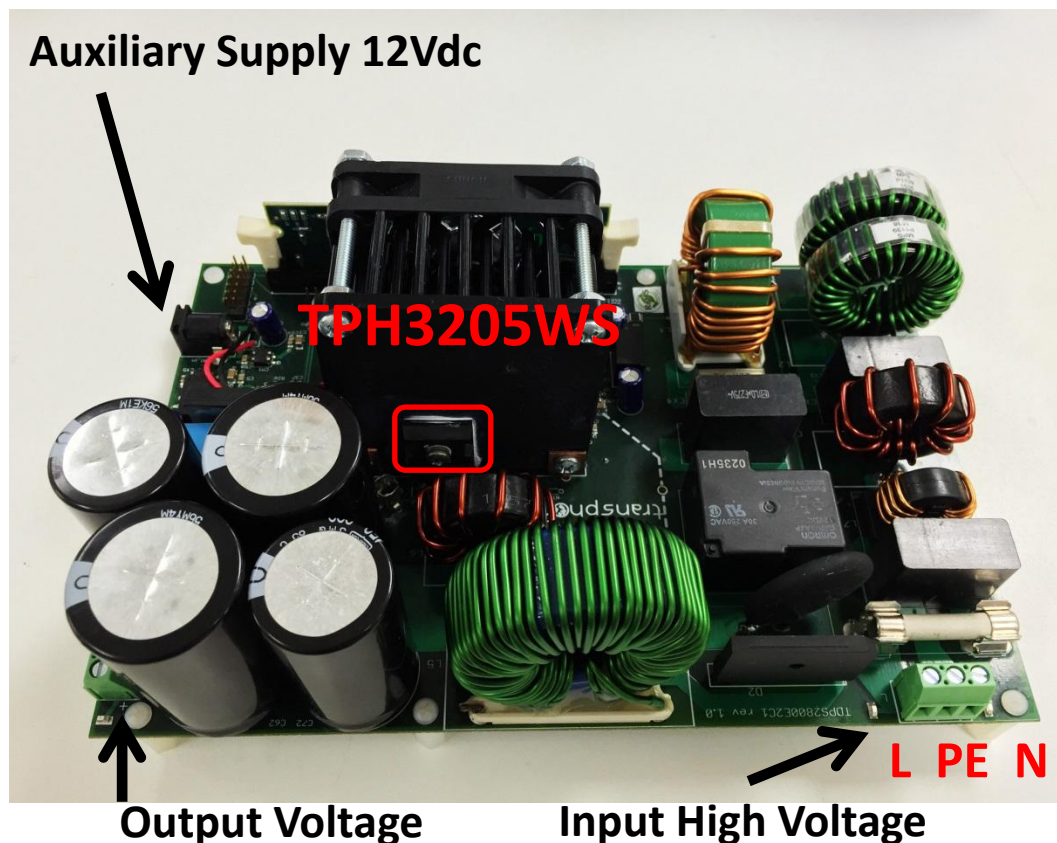


Fig.1a Totem pole PFC Evaluation Board Side 1



Fig.1b Totem pole PFC Evaluation Board Side 2

## 2. TDPS2800E2C1 Input/output Specifications:

- Input voltage: 85 Vac to 260 Vac;
- Input current: 12.6 A (rms) (1400 W at 115 Vac, 2800 W at 230 Vac);
- Output: 390 Vdc  $\pm$  5 V;
- PWM Frequency: 100 kHz;
- Auxiliary Supply (12 Vdc for bias voltage).

## 3. Circuit Description for Totem pole bridgeless PFC based on GaN HEMT

The totem-pole bridgeless topology is shown in Fig. 2. As shown in Fig. 2(a), two GaN HEMT and two diodes are used for the line rectification, while in Fig. 2(b), the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs to eliminate diode drops and improve the efficiency. Further information and discussion on the performance and the characteristics of bridgeless PFC circuit is provided in [1].

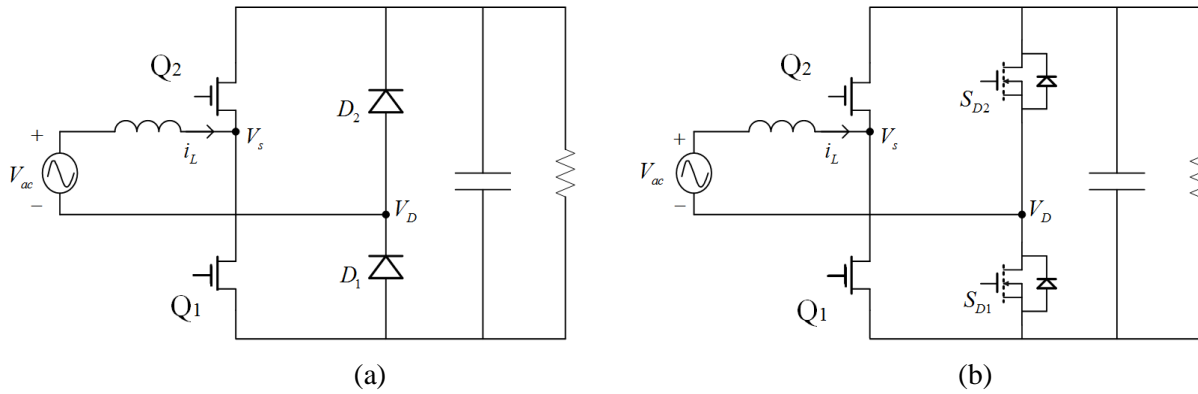


Fig.2 Totem-pole bridgeless PFC boost converter based on GaN HEMT (a) Diode for line rectification (b) MOSFET for line rectification

The large reverse recovery charge ( $Q_{rr}$ ) of existing silicon MOSFETs makes CCM operation of a silicon totem-pole bridgeless PFC impractical, and reduces the total efficiency.

Table 1 gives a comparison of CoolMOS and GaN HEMT.

Table 1: Comparison of GaN HEMT with equivalent CoolMOS IPP60R190C6

Parameter	TPH3205WS	IPW60R099C6
ID	36A	37.9A
Ron	52mΩ	99mΩ
Qg	19nC	119nC
Qrr	136nC	13uC

A GaN HEMT totem pole PFC in CCM mode focusing on minimizing conduction losses was designed with a simplified schematic shown in Fig.4(a). It consists of a pair of fast GaN HEMT switches ( $Q_1$  &  $Q_2$ ) operating at a high pulse-width-modulation (PWM) frequency and a pair of

slow but very-low resistance MOSFETs ( $S_1$  &  $S_2$ ) operating at a much slower line frequency (60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of  $S_1$  &  $S_2$  is that of a synchronized rectifier as illustrated in Fig.4(b) and Fig.4(c). During positive ac cycle,  $S_1$  is on and  $S_2$  off, forcing the ac neutral line tied to the negative terminal of the dc output. The opposite applies for the negative cycle.

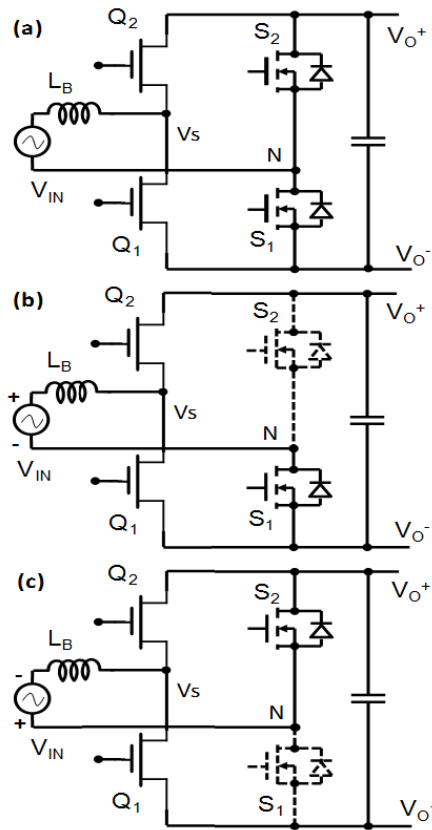


Fig. 4. GaN totem pole PFC (a) simplified schematics and illustration during (b) positive ac cycle and (c) negative ac cycle.

In either ac polarity, the two GaN HEMTs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor ( $L_B$ ) and another transistor as a slave switch to release energy to the dc output. The roles of the two GaN devices interchange when the polarity of the ac input changes; therefore, each transistor must be able to

perform both master and slave functions. To avoid shoot through, a dead time is built in between two switching events during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor has to function as a flyback diode for the inductor current to flow during dead time. The diode current however, has to quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem pole PFC which previously led to abnormal spikes, instability and associated high switching losses due to the high  $Q_{rr}$  of the body diode in modern high-voltage Si MOSFETs. The low  $Q_{rr}$  of the GaN switches allow designers to overcome this barrier. As seen in Fig. 5, inductive tests at 430-V bus using either low-side or high-side GaN transistor as a master switch show healthy voltage waveforms up to inductor current exceeding 25 A. With a design goal of 2.3 kW output power in CCM mode at 230V ac input the required inductor current is 14.7 A. This test conforms a successful totem-pole power block with enough current overhead.

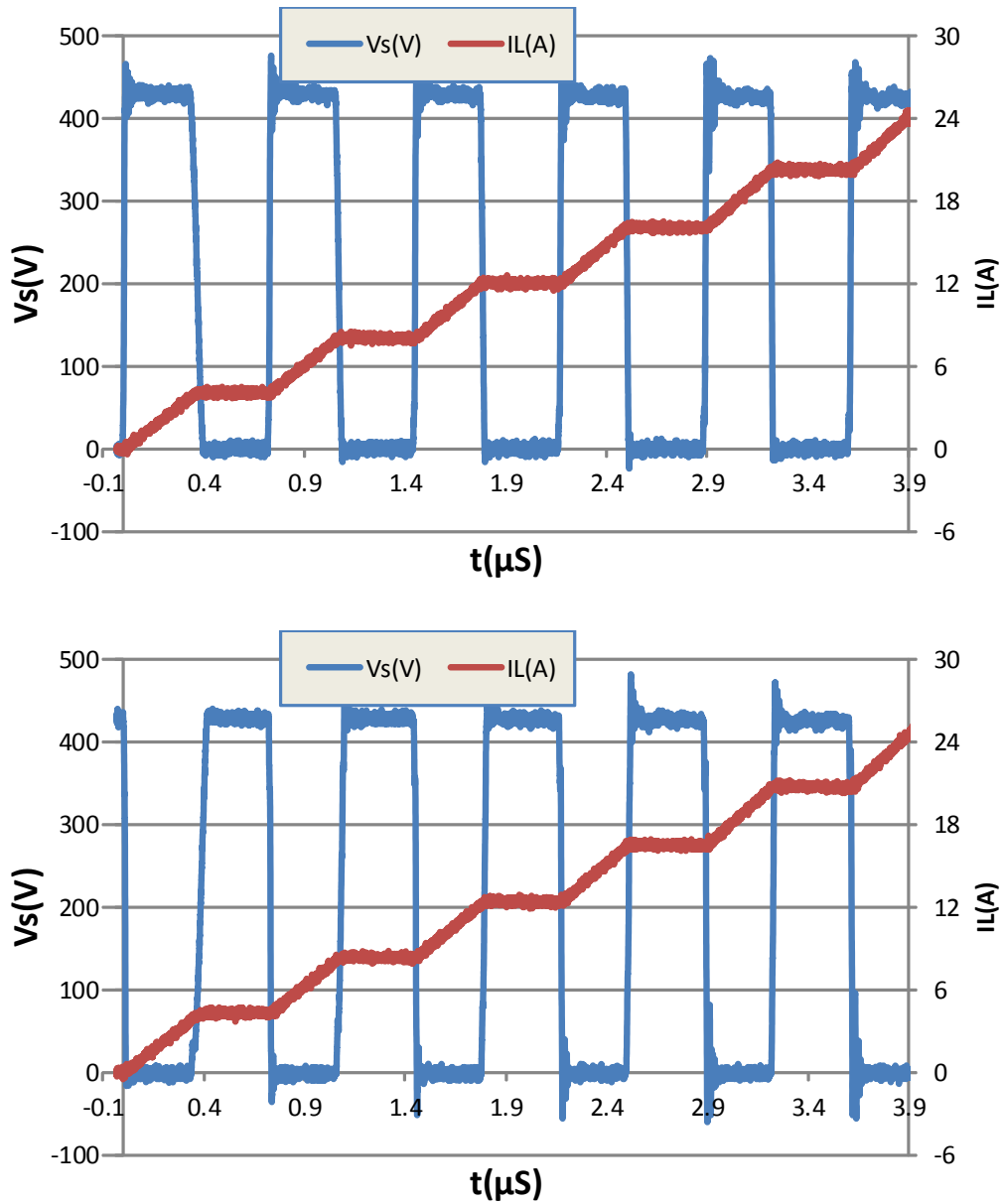


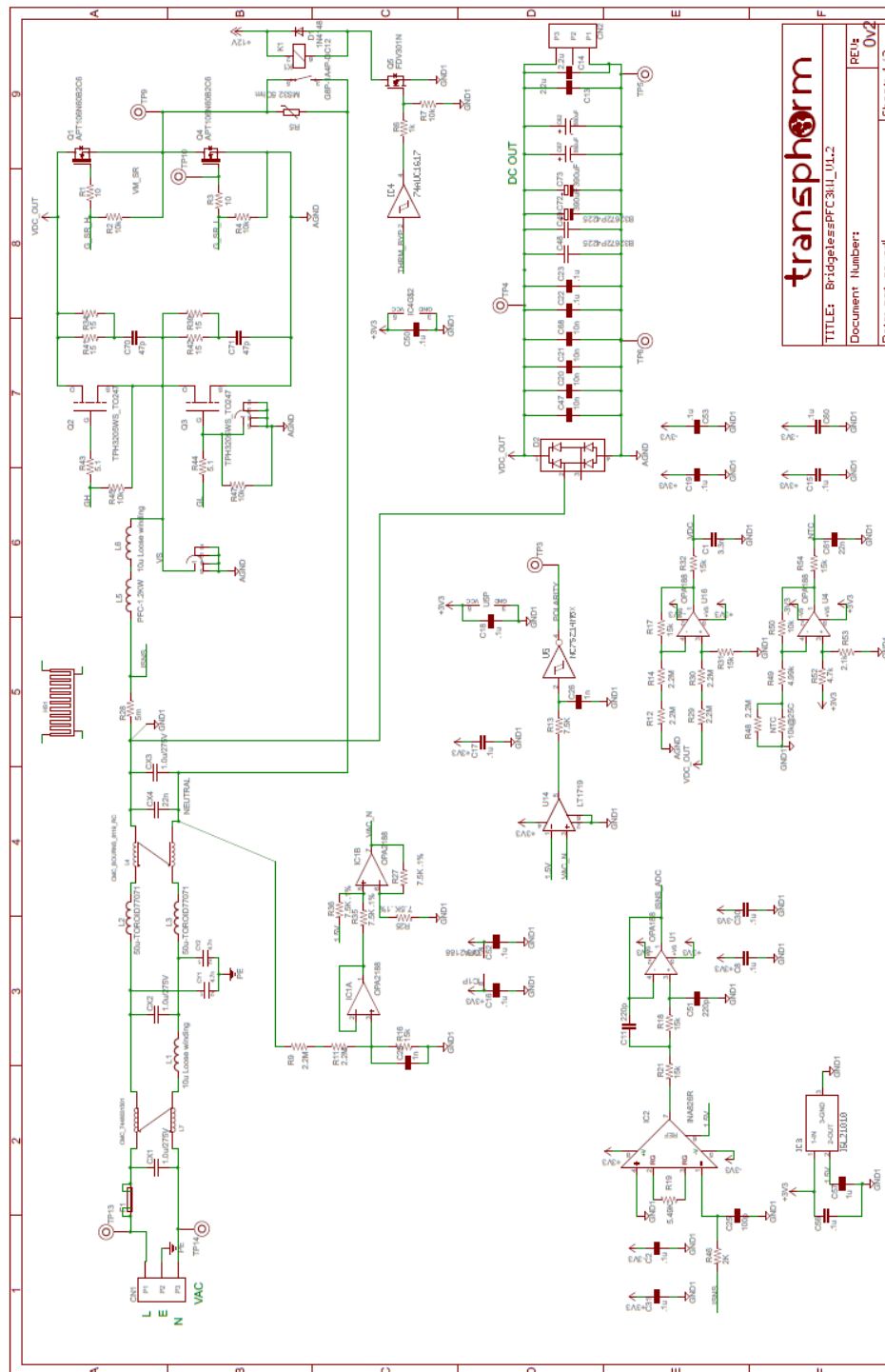
Fig.5 Hard-switched waveforms of a pair of GaN HEMT switches when setting a) high side as master device and b) low side as master

One inherent issue in totem-pole bridgeless PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half line to negative half line at the zero-crossing, the duty ratio of switch Q1 changes abruptly from almost

100% to 0%, and the duty ratio of switch Q2 changes from 0% to 100%. Due to the slow reverse-recovery of diodes (or body diode of MOSFET), the voltage  $V_D$  cannot jump from ground to  $V_{DC}$  instantly, a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio. Since the TDPS2400E2C1 totem-pole bridgeless PFC is designed to run in CCM, the larger inductance actually alleviates the current spike issue at zero-crossing. A soft-start time for a few switching cycles is enough to handle this problem.

The circuit schematic and bill of materials for totem-pole bridgeless PFC evaluation board are shown in Fig. 6 and Table.2 respectively. The schematic is also provided as a separate pdf file with the kit.

For this evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN HEMT half-bridge is built with TPH3205WS devices by Transphorm, Inc. The slow Si switches are STY105NM50N super junction MOSFETs with 0.019 ohm on-resistance. The inductor is made of a Changsu HS core with inductance of 400 uH and a dc resistance 40 mΩ, designed to operate at 100 kHz. A simple 0.5-A rated high/low side driver IC with 0/12 V as on/off states directly drives each GaN HEMT. A 150 MHz DSP – the TMS320F28335 - handles the control algorithm. The voltage and current loop control is similar to conventional boost PFC converter. The feedback signals are dc output voltage ( $V_O$ ), ac input potentials ( $V_{ACP}$  and  $V_{ACN}$ ) and inductor current ( $I_L$ ). The input voltage polarity and RMS value are determined from  $V_{ACP}$  and  $V_{ACN}$ . The outer voltage loop output multiplied by  $|V_{AC}|$  gives sinusoidal current reference. The current loop gives the proper duty-ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive  $Q_1$  &  $Q_2$ . A soft-start sequence with a duty ratio ramps is employed for a short-period at each ac zero-crossing for better stability.





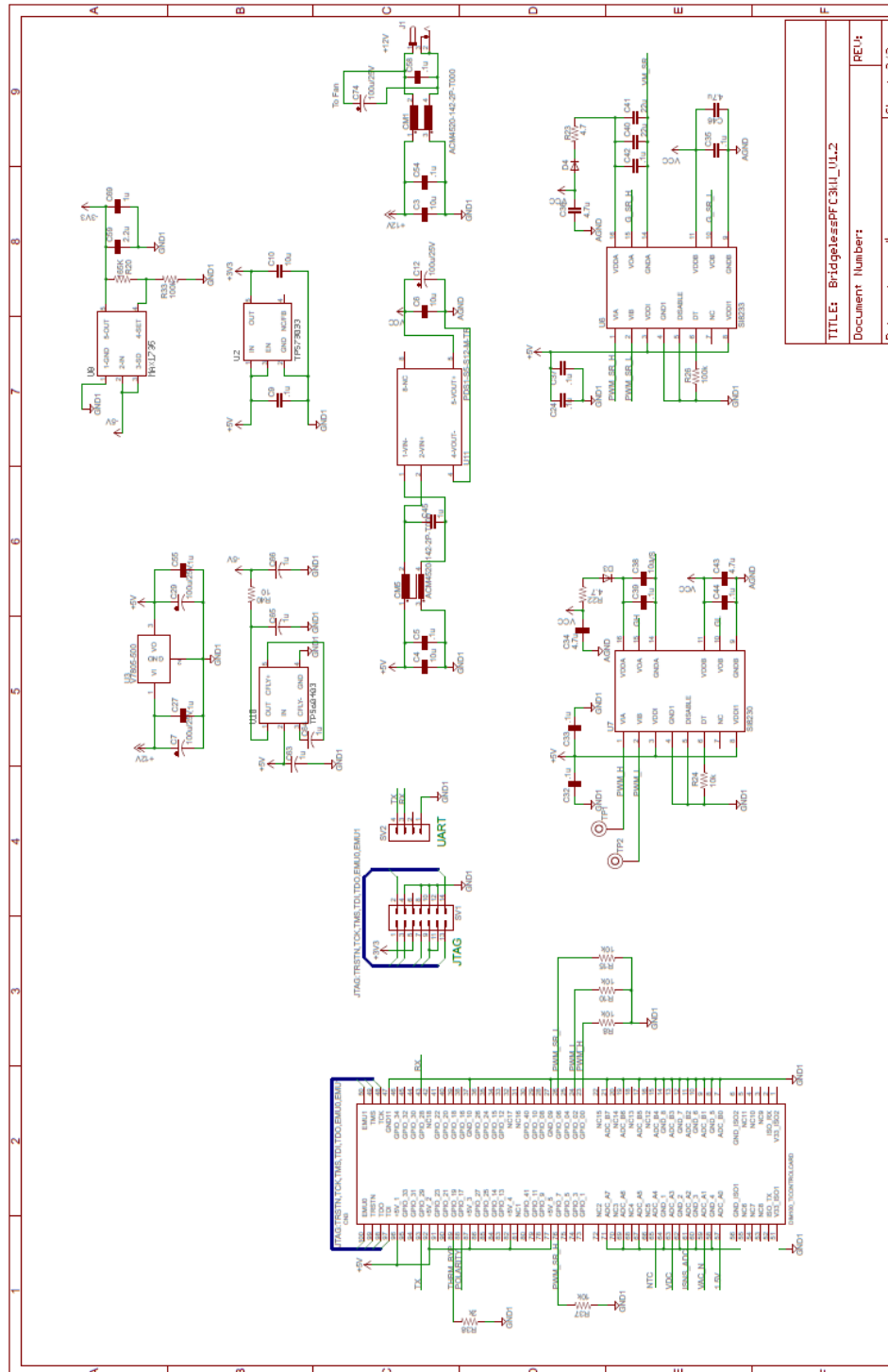


Fig.6. Totem Pole PFC Evaluation Board Schematics

Table.2. Bill of Materials

Qty	Value	Device	Parts	Manf	Manf P/N
1	60mm x 60mm	3-242411MS73377	HS1	Cool Innovation	529802B02500G
2	1A/600V	DIODE-DO-214AC	D3, D4	Micro Commercial	ES1J
2	10A/600V	FCI_20020316-3P	CN1, CN2	FCI	20020316-H031B01LF
1	25A/600V	GBJ2506	D2	Micro Commercial	GBJ2506-BP
1		MA04-1	SV2	3M	961104-6404-AR
1		MA07-2	SV1	FCI	67996-114HLF
1	Fuse holder	SH32	F1	LITTLE FUSE	01020078H
2		TEKTRONIX-PCB	TP7, TP8	Tektronix	131-4353-00
12		TESTPOINT-KEYSTONE5015	TP1, TP2, TP3, TP4, TP5, TP6, TP9, TP10, TP11, TP12, TP13, TP14	Keystone	5015
15	.1u/16V	C-EUC0603	C2, C8, C15, C16, C17, C18, C19, C30, C31, C35, C44, C52, C53, C56, C60	Kemet	C0603C104J3RACTU
14	.1u/16V	C-EUC0805	C5, C9, C24,	AVX	08053C104KAT2A

			C27, C32, C33, C37, C39, C42, C50, C54, C56, C55, C58		
2	.1u/1kV	C-EUC1812	C22, C23	Kemet	C1812V104KDRACTU
2	5.1	R-US_R0805	R43, R44	Stackpole	RMCF0805JT10K0
3	1.0u/275V 20%	ECQ- U2A474ML1.0U	CX1, CX2, CX3	Panasonic	ECQ-U2A105ML
1	1N4148	DIODE-SOD123	D1	Vishay	1N4148W-E3-18
1	1k	R-US_R0805	R6	Panasonic	ERJ-6ENF1001V
2	1n/50V	C-EUC0805	C26, C28	Yageo	CC0805KRX7R9BB102
3	1u/25V	C-EUC0805	C45, C57, C69	Yageo	CC0805ZRY5V8BB105
4	1u/25V	C-USC0603	C63, C64, C65, C66	Taiyo Yuden	TMK107B7105KA-T
6	2.2M	R-US_R1210	R9, R11, R12, R14, R29, R30	Rohm Semiconductor	KTR25JZPF2204
2	4.7n/400V AC	PHE850YCAP	CY1, CY2	Kemet	C947U472MYVDBA73 17
1	2.2u/25V	C-EUC1206	C59	Samsung Electro	CL31B225KAHNNNE
1	2k	R-US_R0805	R38, R46	Panasonic	ERJ-6ENF2001V
1	3.3n/50V	C-EUC0805	C1	Kemet	C0805C332K5RACTU
1	5.5K	R-US_R0805	R19	Susumu	RR1220P-5491-D-M

2	4.7	R-US_R1206	R22, R23	BOURNS	CRM1206-JW-4R7ELF
4	4.7u/16V	C-EUC1206	C34, C36, C43, C46	Kemet	C0805C475K4PACTU
1	5m	R-US_0613/15	R28	Ohmite	12FR005E
1	7.5K	R-US_R0805	R13	Panasonic	ERJ-6ENF7501V
4	7.5K .1%	R-US_R0805	R25, R27, R35, R36	Panasonic	ERA-6AEB752V
4	15	R-US_R1206	R34, R39, R41, R42	Stackpole	RNCP1206FTD15R0
3	10n/630V	C-EUC1206	C20, C21, C47	TDK	CGA5L4C0G2J103J160 AA
2	10	R-US_R0805	R1, R3	Panasonic	ERJ-6GEYJ100V
1	10	R-US_R1206	R40	Panasonic	ERJ-8ENF10R0V
11	10k	R-US_R0805	R2, R4, R7, R8, R10, R15, R24, R37, R45, R47, R50	Panasonic	ERJ-6ENF1002V
5	10u/25V	C-EUC1206	C3, C4, C6, C10, C38	AVX	12063D106KAT2A
2	10u Loose winding	DM-TOROID	L1, L6		
7	15k	R-US_R0805	R16, R17, R18, R21, R31, R32, R54	Yageo	05FR-0715KL
1	22n/275V AC	ECQ-U2A474ML22N	CX4	Kemet	PME271M522MR30

2	22u/25V	C-EUC1206	C40, C41	Samsung Electro	CL31X226KAHN3NE
2	47p/1kV	C-EUC1210	C70, C71	Vishay	VJ1210A470JXGAT5ZL
2	50u-TOROID77071	DM-TOROID77071	L2, L3		
1	74AUC1G17	74AUC1G17DBV	IC4	Texas Instruments	SN74LVC1G17DBVR
2	100k	R-US_R0805	R26, R33	Panasonic	RJ-6ENF1003V
1	100p/50V	C-EUC0603	C25	AVX Corporation	06035A101FAT2A
3	100u/25V	CPOL-USE2.5-7	C7, C12, C29	Kemet	ESK107M025AC3AA
1	165K	R-US_R0805	R20	Panasonic	ERJ-6ENF1653V
2	220p/50V	C-EUC0805	C11, C51	Yageo	CC0805KRX7R9BB221
2	ACM4520-142-2P-T000	ACM4520	CM1, CM5	TDK	ACM4520-142-2P-T000
2	STY105NM50N	STY105NM50N	Q1, Q4	STMicroelectronics	STY105NM50N
2	2.2uF/450V	B32672P4225	C48, C49	EPCOS (TDK)	B32672P4225K
4	390uF/450V	CPOL	C72, C73, C74, C75	Rubycon	450MXK390MEFCSN25X50
1	DIM100_TICONTROLCARD holder	DIM100_TICONTROLCARD	CN3	Texas Instruments	TMDSDIM100CON5PK
1	FCI_20020316-2P	FCI_20020316-2P	CN7	FCI	20020316-H021B01LF
1	FDV301N	BSS138-7-F	Q5	Fairchild	FDV301N

1	G8P-1A4P-DC12	G8P-1A4P	K1	Omron Electronics	G8P-1A4P-DC12
1	INA826R	INA826R	IC2	Texas Instruments	INA826AID
1	ISL21010	ISL21010	IC3	Intersil	ISL21010CFH315Z-TK
1	LT1719	LT1719	U14	Linear Technology	LT1719CS6#TRMPBF
1	MAX1735	MAX1735	U8	Maxim Integrated	MAX1735EUK50+T
1	MS32 50hm	THERMISTOR-AMETHERM	R5	Ametherm	SL32 10015
1	NC7SZ14M5X	NC7SZ14M5X	U5	Fairchild	NC7SZ14M5X
3	OPA188	OPA188	U1, U4, U16	Texas Instruments	OPA188AIDBVT
1	OPA2188	OPA2188	IC1	Texas Instruments	OPA2188AIDR
1	PDS1-S5-S12-M-TR	PDS1-S5-S12-M-TR	U11	CUI	PDS1-S5-S12-M-TR
1	PFC-1.2KW	PFC-1.2KW	L6	MPS Industries	P1941_A
1	SI8230	SI8230	U7	Silicon Labs	SI8230BB-B-IS1
1	SI8233	SI8233	U6	Silicon Labs	SI8233BB-C-IS1
2	TPH3205WS	TPH3205WS	Q2, Q3	Transphorm	TPH3205WS
1	TPS60403	TPS60403	U10	Texas Instruments	TPS60403DBVR
1	TPS73033	TPS73033	U2	Texas Instruments	TPS73033DBVR

1	V7805-500	V7805-500	U3	CUI	7805-500
1		Power Jack	J1	CUI	PJ-002AH
1	2.1k	R0805	R53	Yageo	RC0805FR-072K1L
1	4.99k	R0805	R49	Panasonic	ERJ-6ENF4991V
1	1mH	Common Mode Choke	L4	BOURNS	8121-RC
1	1mH	Common Mode Choke	L7	Würth Electronics	7448031501
1	2.2M	R0805	R48	Stackpole	RMCF0805JT2M20
1	10k@25C	Bead with Terminal	NTC	EPCOS (TDK)	B57703M103G40

While a typical Si MOSFET has a maximum  $dV/dt$  rating of 50V/ns, the Transphorm GaN HEMT will switch at  $dV/dt$  of 100V/ns or higher to enable the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown below, in Fig. 7-9, the recommended layout keeps a minimum gate drive loop; it also keeps the traces between the switching nodes very short, with the shortest practical return trace to power bus and ground. As the power ground plane provides a large cross sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the HEMT to avoid any possible ground loop.

Note that the Transphorm GaN HEMTs in TO247 package has pin out configured as G-S-D, instead of traditional MOSFET's G-D-S arrangement. The configuration is designed with thorough consideration to minimize the Gate-Source driving loop to reduce parasitic inductance, as well as to separate the driving loop (Gate-Source) and power loop (Drain-Source) to minimize noise. For further information, different layers of TDPS2800E2C1 design are shown in Fig. 8-10.

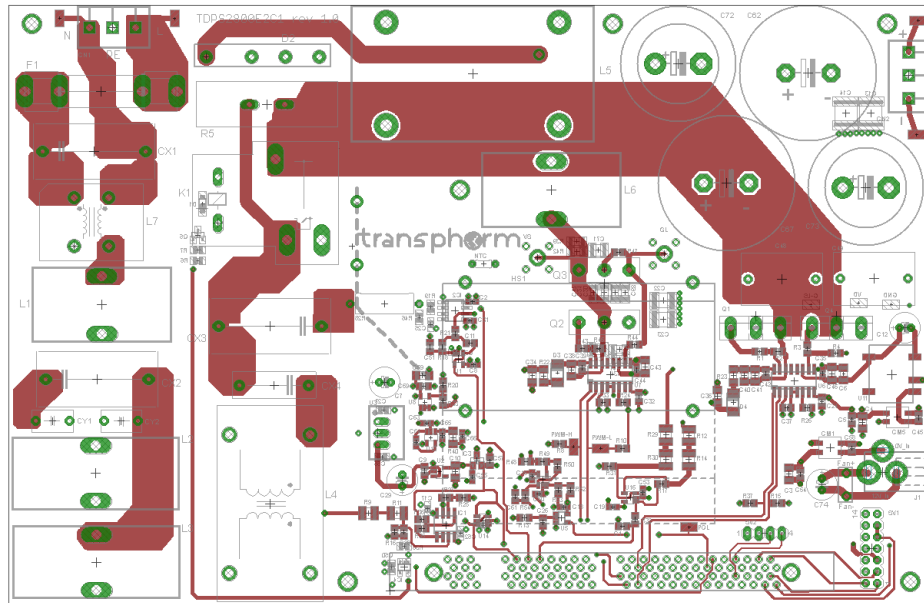


Fig. 7. Totem Pole PFC Evaluation Board Layout, Top Layer

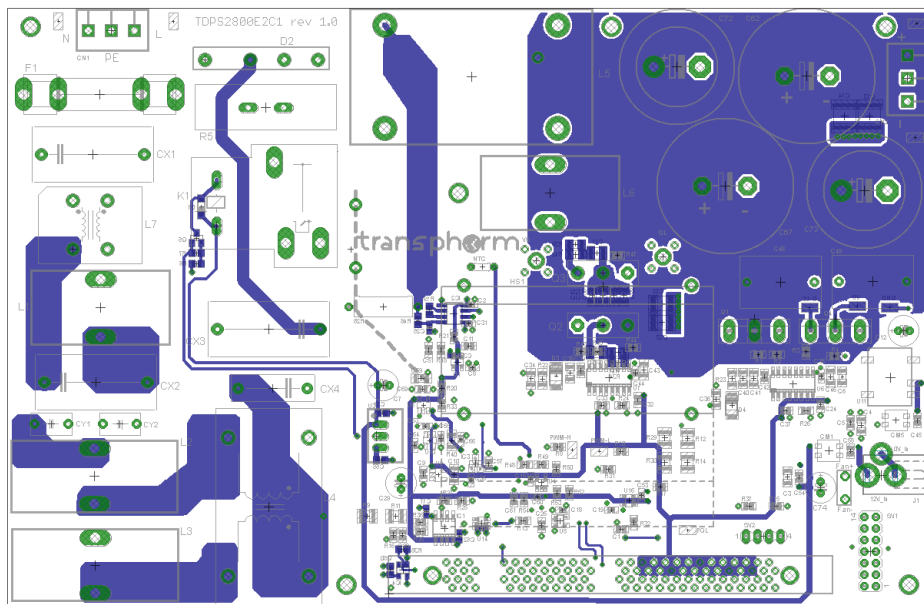


Fig. 8. Totem Pole PFC Evaluation Board Layout, Bottom Layer



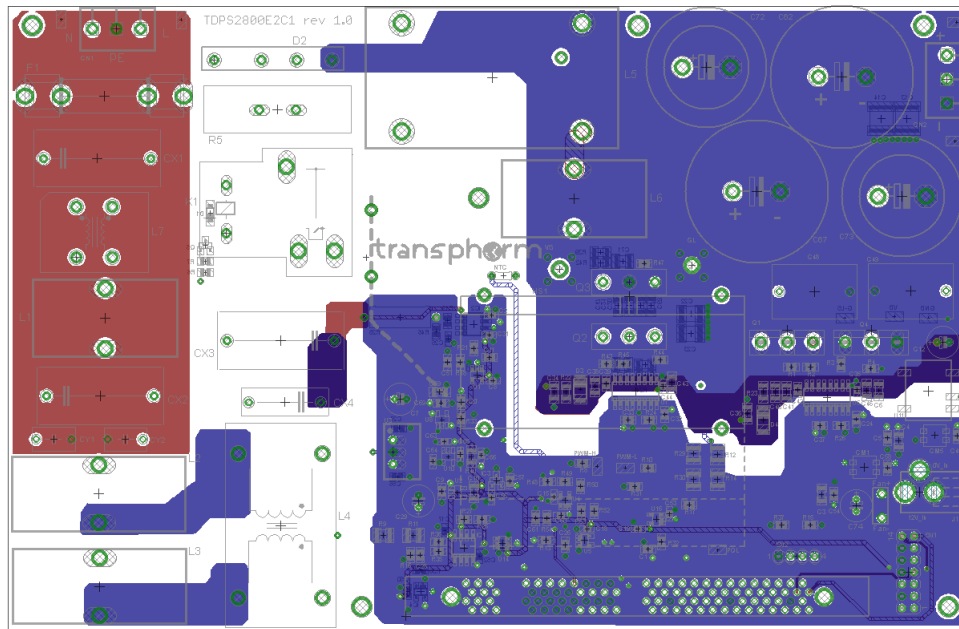


Fig. 9. Totem Pole PFC Evaluation Board Layout, Middle Layers

## Turn on Sequences:

- 1) Connect a load; the load should be resistive.

The requirement for the resistive load:

- At 115 Vac input:  $\geq 200 \text{ W}$  and  $\leq 1400 \text{ W}$
- At 230 Vac input:  $\geq 200 \text{ W}$  and  $\leq 2800 \text{ W}$

- 2) Connect the 12 Vdc auxiliary supply to the demo-board (included in demo-kit package).
- 3) With power off, Connect the high-voltage AC power input to the corresponding marking on the PCB;
- 4) Place a cooling fan facing the PFC inductor and heat sink (provide a minimum of 30 CFM air flow) for full load;
- 5) Turn on the cooling fan.
- 6) Turn on the AC power input (85 Vac to 260 Vac).
  - a. Apply resistive load while AC supply is ON.

## Turn off sequences:

- 1) Switch off the high-voltage AC power input;
- 2) Power off dc bias;
- 3) Turn off the fan.

Fig.10 shows the converter start-up, CH3 shows the DC bus voltage rapidly rising with simple rectification at the beginning and then ramping up to 390V under control, while the inductor current is kept under control during the start-up process.

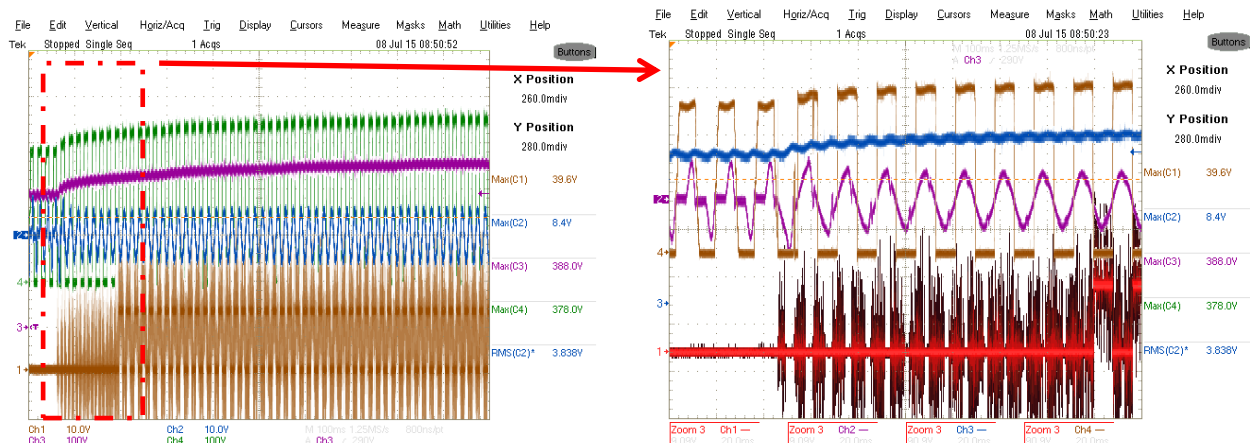


Fig.10 Start-up of the totem-pole bridgeless PFC prototypes (CH1: Vg, CH2: iL, CH3: Vo, CH4: Vd)

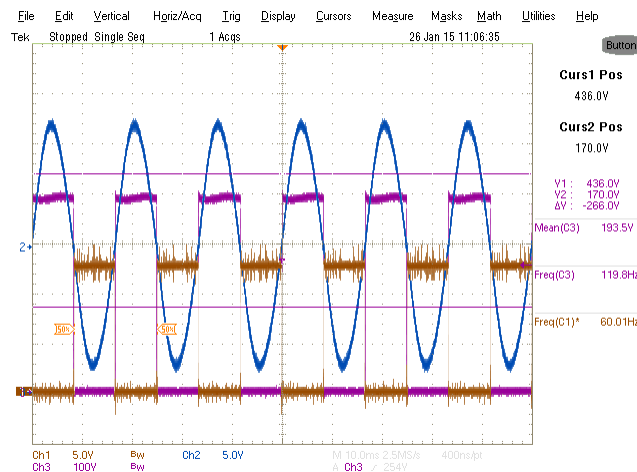


Fig.11 Waveform of the active switch version of the totem-pole bridgeless PFC at low line, full load; (a) CH1: PWM Gate signal for  $S_{D2}$ ; CH2:  $I_L$  waveform (10A/division); CH3:  $V_D$  waveform (100V/division); CH4: AC input polarity signal

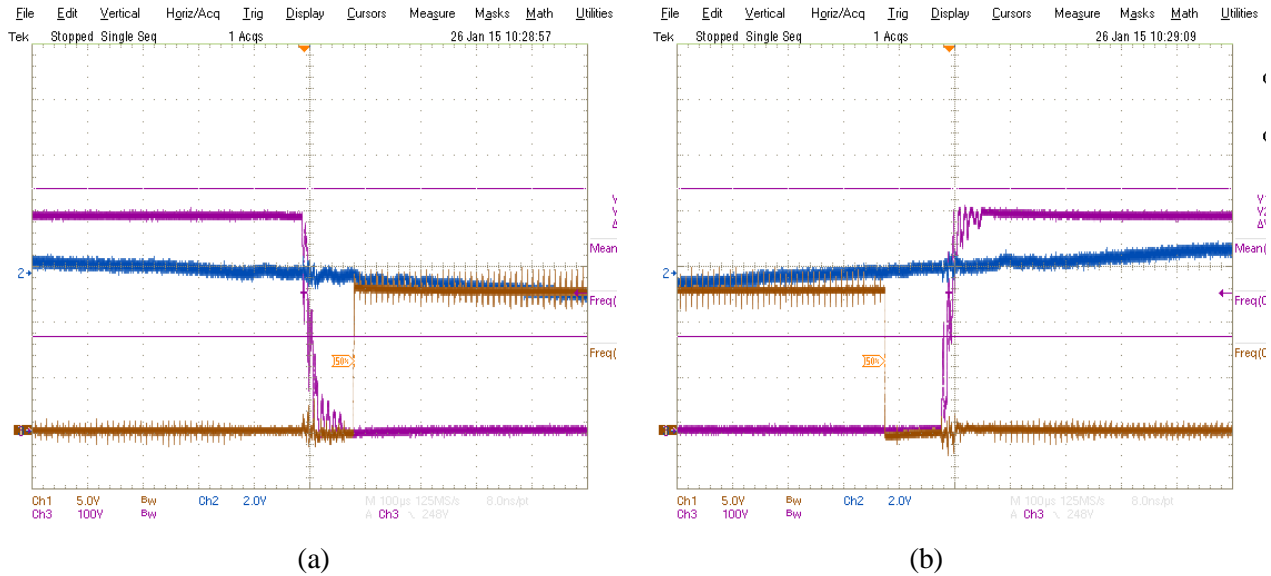


Fig. 12 Zero-crossing transitional waveform (a) from negative to positive half cycle (b) from positive to negative half cycle. CH1: PWM Gate signal for  $S_{D2}$ ; CH2:  $I_L$  waveform; CH3:  $V_D$  waveform.

Fig.12 shows the transitions between two half cycles. In Fig.12(a), the AC line enters the negative half. Soft-start gradually increases voltage  $V_D$  from 0V to 390 V. While in Fig. 12(b),  $V_D$  decreases from 390 V to 0 V.

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at 115 Vac or 230 Vac input and 400 Vdc output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this Totem Pole PFC board are shown in Fig.13. The extremely high efficiency of 98.8% at 230Vac input, and >97.5% at 115V ac input is the highest among PFC designs with similar PWM frequency; this high efficiency will enable customers to reach peak system efficiency to meet and exceed Titanium standards.

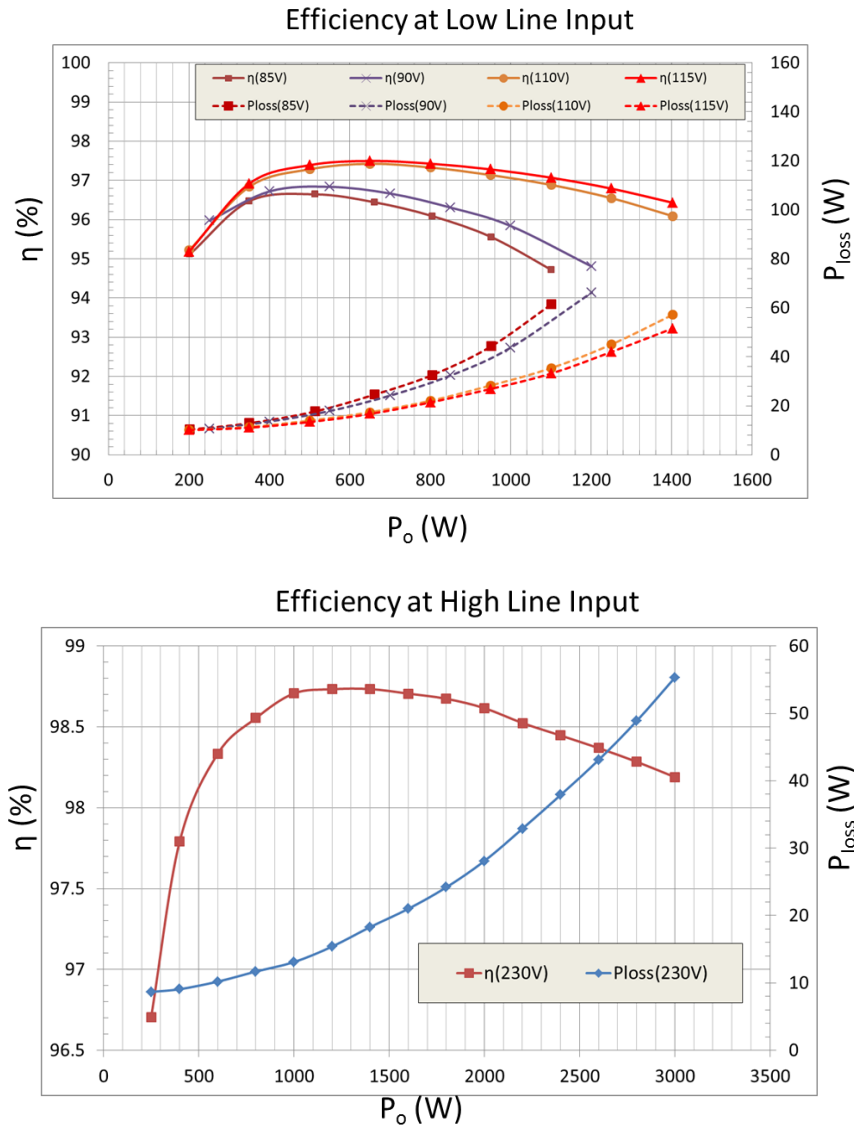


Fig. 13. The efficiency result for Totem Pole PFC board

Conducted emissions have also been measured for this board using a LIN-115A LISN by Com-Power. Put the ferrite core clamps on both input cable and output cable (included in Demo Kits). The results compared to EN55022B limits are show in Fig. 14. It should be noted that the EMI test was done by using lab-use power supply for auxiliary 12V source. **Do not use wall AC-DC adaptor for EMI test.**

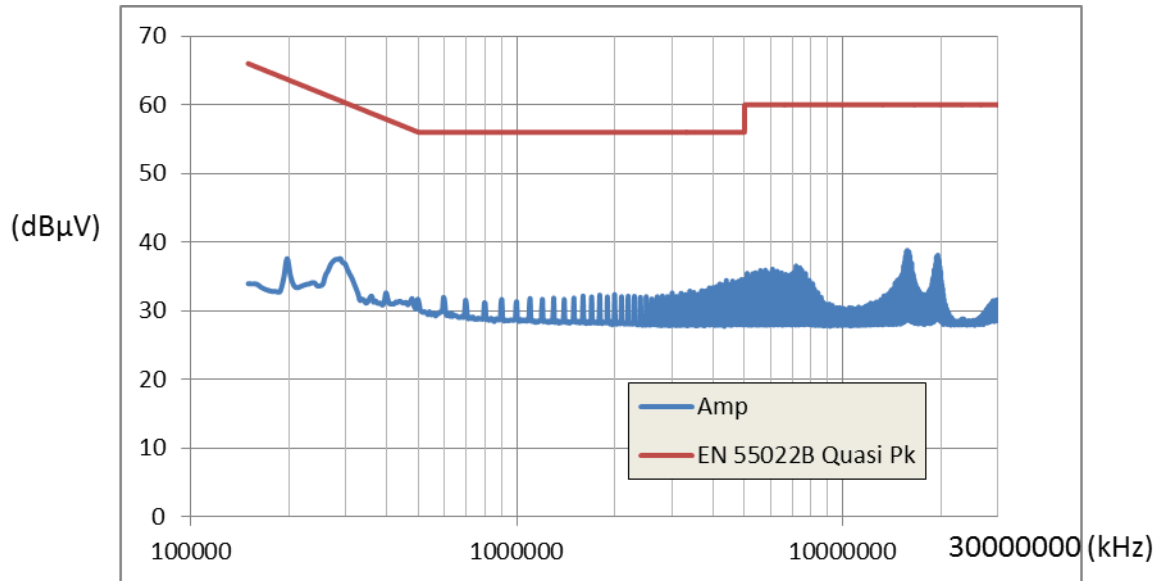


Fig. 14. Conducted emissions @115V, 680W

## Maximum Load Limit:

TDPS2800E2C1 totem pole is allowed to run overload with strong additional forced air in short time. Fig. 15 shows the load limit in various input voltage. It allows running overload in short time with strong forced air cooling.

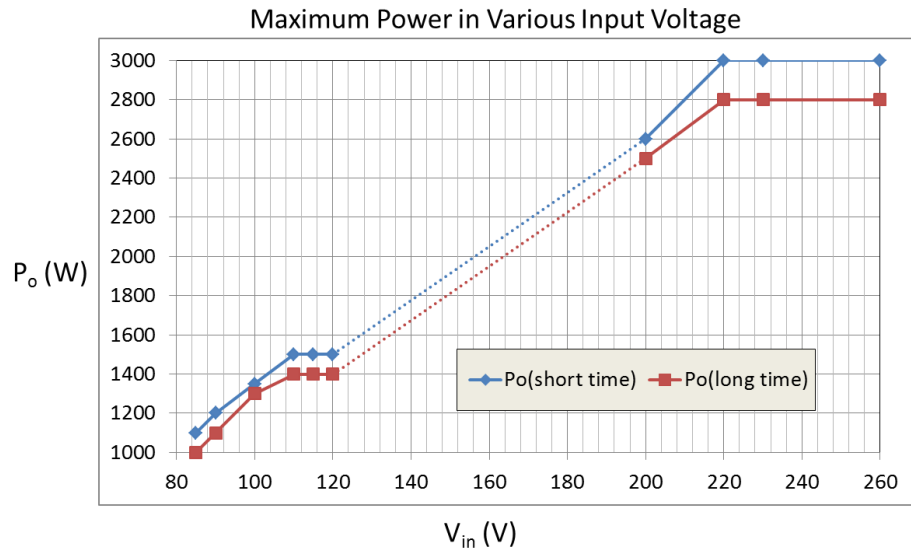


Fig. 15. Maximum Power Allowance in Various Input Voltage

**⚠Warning:**

This demo board is intended to demonstrate GaN HEMT technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. An isolated AC source should be used as input; an isolated lab bench grade power supply or the included AUX DC supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.
2. Use a resistor load only. The Totem-pole PFC kit also has a minimum load requirement. It **DOES NOT** work at no load.
3. The demo board is not intended to handle large load steps. **DO NOT** apply a large step in the load (>1000W) when it is running.
4. **DO NOT** manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.
5. The auxiliary Vcc supply must be 12 V. The demo board will not work under, for example 10 V or 15V Vcc.
6. **DO NOT** touch any part of the demo board when it is running.
7. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.
8. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.

9. **DO NOT** use passive probe to measure control circuit signals and power circuit signals in the same time. GND1 and AGND are not the same ground.

## REFERENCE:

- [1]. Liang Zhou, Yi-Feng Wu and Umesh Mishra, “True Bridgeless Totem-pole PFC based on GaN HEMTs”, PCIM Europe 2013, 14-16 May, 2013, pp.1017-1022.
- [2]. L. Huber, Y. Jang, and M. M. Jovanovic, “Performance evaluation of bridgeless PFC boost rectifiers,” IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp. 1381-1390, May 2008.