GaN Totem-pole PFC: The Most Elegant Active Power Factor Correction Circuit Eliminating Diode Drop

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ABSTRACT: *The advent of high-voltage GaN power transistors allows unconventional circuits previously impractical to implement. The simultaneously low on-resistance and low reverse recovery charge from the 1st-generation GaN-on-Si HEMT offer a new keystone in building a long-awaited totem pole power correction circuit (PFC). In addition to excellent potential for low common-mode EMI noises, this elegant GaN-based PFC features the least number of fast power devices and offers the least resistance path for the main current, enabling a prototype to achieve 99% efficiency from a 230V ac line to 400V dc bus.*

[INTRODUCTION] While it is desired that new device technologies continuously improve performance of popular circuits, it is of higher impact if a development enables new functions and revives a dormant topology to outperform its prevailing counterparts. Active Power Factor Correction (PFC) circuit has widespread use and is getting even more popular as government agencies demand more effective use of grid supply capacities. A typical PFC includes a diode bridge for rectifying the ac source and a boost stage to force the input current proportional to the input voltage. The rectifier bridge consumes a significant part of the circuit loss hence many topology innovations for bridge-less PFCs emerged. Most of them suffer from either common-mode (CM) Electromagnetic noise (EMI) or other issues therefore are not practical. One unique topology called the totem pole PFC has both simple power loops and the low CM noise feature [1]. However, it demands very-low reverse recovery charges (Qrr's) for the MOSFET body diodes, which were not available hence no good hard-switched totem pole PFC was ever made. With the advent of GaN power devices [2] [3], 600V-class low Qrr transistors are now available to enable this highly promising circuit.

[PFC TOPOLOGY REVIEW] The evolution of representative PFC topologies is shown in Fig.1. A traditional PFC (Fig.1a) consists of a slow-recovery full-bridge line rectifier (D_1-D_4), a fast boost diode (D_B) and a fast transistor switch (S_B). In addition to D_B or S_B, the main current passes 2 of the 4 slow diodes at a given time, which can account for an efficiency loss by 0.6% to 1.2% (at high line and low line respectively) due to the forward diode drop.

The basic bridge-less PFC shown in Fig. 1b) eliminates all slow diodes, but requires two fast diodes (D_{B1} & D_{B2}) and two fast switches (S_{B1} & S_{B2}) [4]. The main current path includes only one switch plus either one diode or another switch, capable of a significantly higher efficiency. However,

both ac input nodes during the negative ac cycle are floating with respect to the two dc output terminals, leading to a high CM EMI noise [5]. For this reason this topology has limited practical use.

Attempts were made to modify the basic bridge-less PFC for lower CM noises. A successful example is the dual-separate-boost bridge-less PFC shown in Fig. 1c) [6]. Employing two boost inductors (L_{B1} & L_{B2}), two fast diodes (D_{B1} & D_{B2}) and two fast transistors (S_{B1} & S_{B2}) in addition to two slow-recovery rectifying diodes (D_1 & D_2), this PFC ensures the potential of one ac input node to be effectively tied to an dc output terminal at any given time; hence significantly reduces CM noises and has earned popularity among power circuit designers [7]. However, this circuit requires the largest number of fast devices (D_{B1}, D_{B2}, S_{B1} & S_{B2}) and inductors (L_{B1} & L_{B2}), yet eliminates only one diode drop compared to the traditional PFC in Fig. 1a).

Fig. 1d) shows the totem pole bridgeless PFC with two fast devices (S_{B1} & S_{B2}), one inductor (L_B) and two low-cost slow diodes (D_1, D_2). The ability to ensure low CM noises is realized by the fact that one ac node is always clamped by a slow diode to either the top or bottom of the two dc output terminals. Additionally, no voltage drop of a fast diode is involved, offering potential for further efficiency enhancement. The difficulty to implement this circuit lies in the fact that during dead-time when both transistor switches are off, one of the body diode is turned on to allow free-wheeling current in continuous current mode (CCM) operation. In the subsequent hard-switching event, the Qrr of the body diode in high-voltage Si MOSFETs could cause huge current-voltage spikes, making the circuit unstable in addition to high switching losses. The key to enable a successful totem pole PFC relies on new generation semiconductors with simultaneously low on-resistance and low recovery charge.

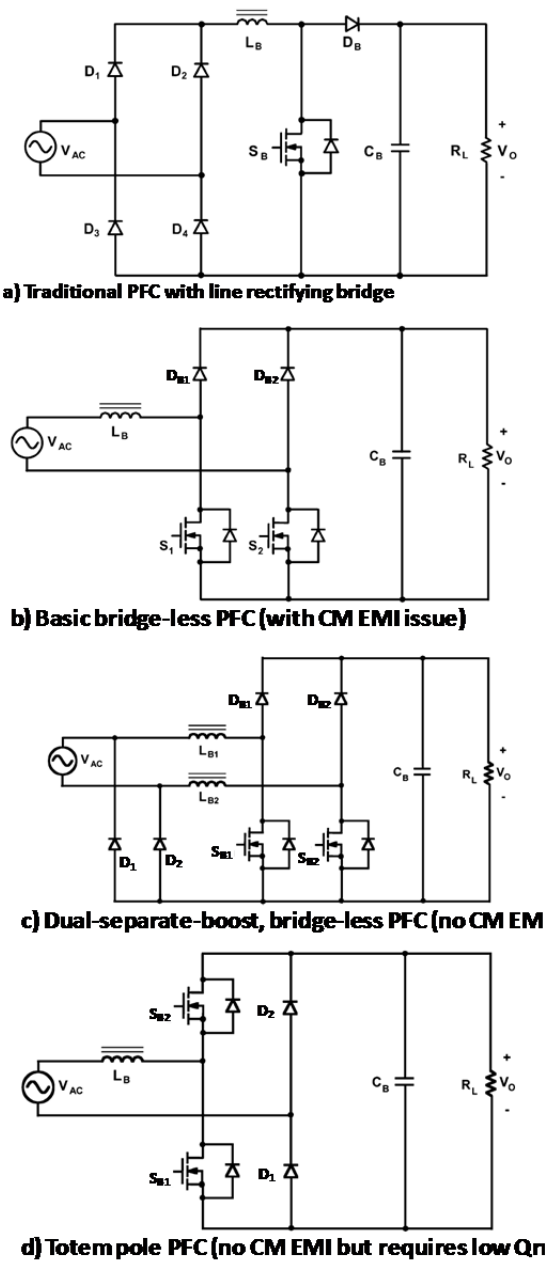

Fig.1 Representative PFC topologies: a) traditional, b) basic bridge-less, c) dual-separate-boost and d) totem pole.

[**GaN TOTEM POLE PFC**] Industry's 1st qualified 600-V GaN HEMTs made on low-cost Si substrate has been announced by Transphorm Inc.. These 1st-generation GaN power devices show a low on-resistance of 0.15 ohm typical and are capable of reverse conduction during dead time with a low Qrr of 54 nC, 20 times lower than state-of-the-art Si counterpart as seen in Fig.2. These features can remarkably expand operation space of a hard-switched bridge. Moreover, these devices are offered in Quiet-tab™ configurations with choices of the metal tab connected to the drain or source terminals. When a drain tab package is used for the high-side device (e.g. S_{B2} in Fig. 1) and a source tab as low-side device (e.g. S_{B1} in Fig. 1), the capacitive coupling between device and heat sink is minimized, further reducing EMI noises. A GaN HEMT totem pole PFC in CCM mode focusing on minimizing conduction losses was designed with a simplified schematic shown in Fig.3 (a). It consists of a pair of fast GaN HEMT switches (Q_1 & Q_2) operating at a high pulse-width-modulation (PWM) frequency and a pair of slow but very-low resistance MOSFETs (S_1 & S_2) operating at a much slower line frequency (60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S_1 & S_2 is that of a synchronized rectifier as illustrated in Fig.3 a) and b). During positive ac cycle, S_1 is on

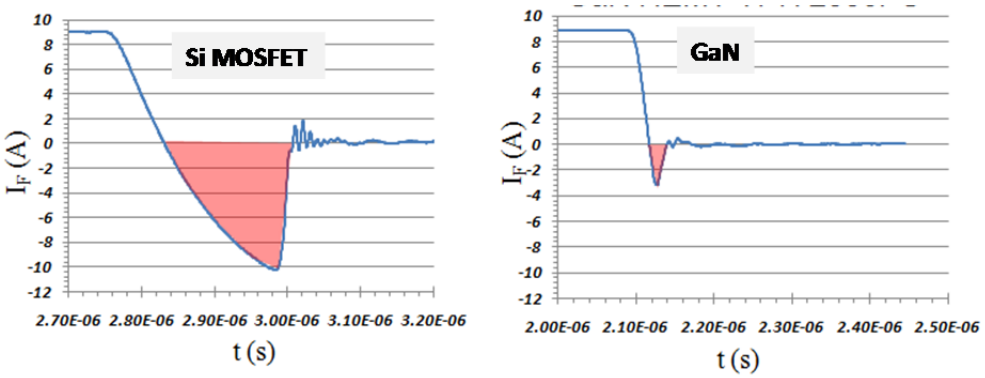

Fig.2 Reverse recovery charge test result for a Si MOSFET and a GaN HEMT with similar on resistance, showing a 20x reduction of Qrr for GaN.

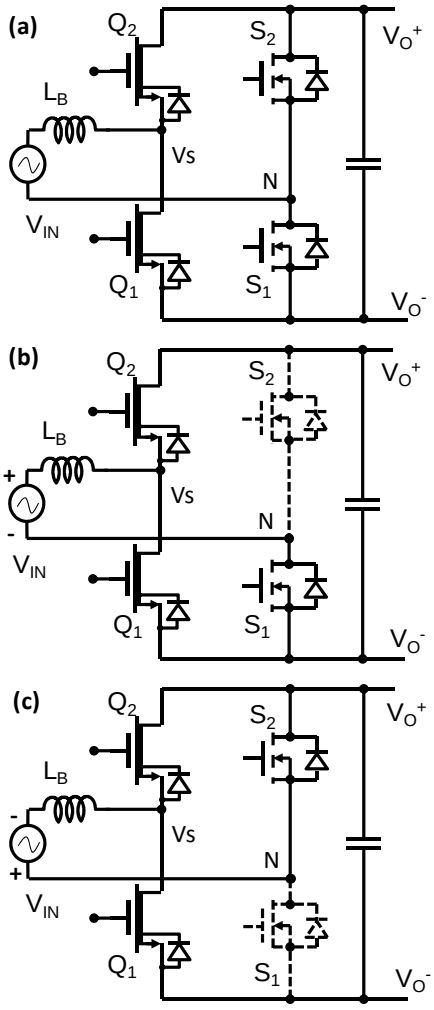

Fig.3 GaN totem pole PFC (a) simplified schematics and illustration during (b) positive ac cycle and (b) negative ac cycle.

and S_1 off, forcing the ac neutral line tied to the negative terminal of the dc output. The opposite applies for the negative cycle.

In either ac polarity, the two GaN HEMTs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (L_B) and another transistor as a slave switch to release energy to the dc output. The roles of the two GaN devices interchange when the polarity of the ac input changes, therefore each transistor must be able to perform both master and slave functions. To avoid shoot through, a dead time is built in between two switching events during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor has to function as a free-wheeling diode for the inductor current to flow during dead time. The diode current however, has to quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem pole PFC which previously led to abnormal spikes, instability and associated high switching losses due to the high Qrr of the body diode in modern high-voltage Si MOSFETs. The low Qrr of the GaN switches allow designers to overcome this barrier. As seen in Fig. 4, inductive tests at 400-V bus using either low-side or high-side GaN transistor as a master switch show healthy voltage waveforms up to inductor current exceeding 12 A. With a design goal of 1 kW output power in CCM mode at 230V ac input the required inductor current is 6 A. This test conforms a successful totem-pole power block with 2x current overhead.

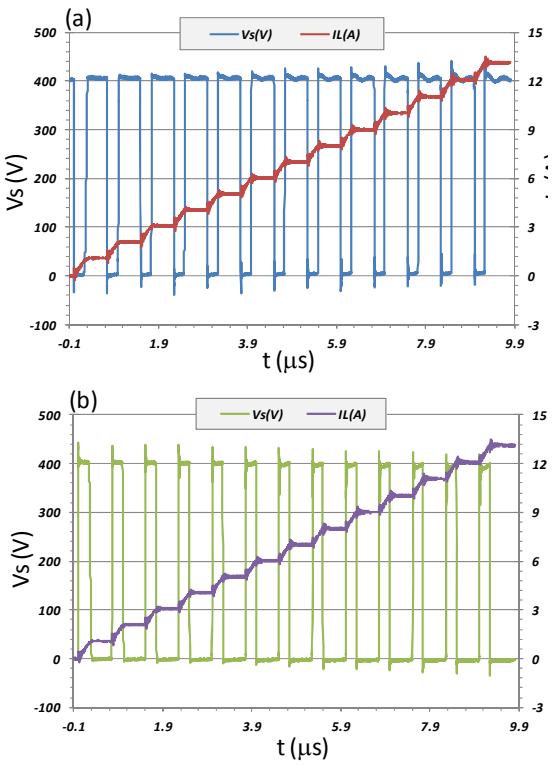

Fig.4 Hard-switched waveforms of a pair of GaN HEMT switches when setting a) low side as master device and b) high side as master.

[PFC PROTOTYPE & PERFORMANCE] The PFC has been implemented on a 4-layer PCB as shown in Fig. 5. The slow switches (S_1

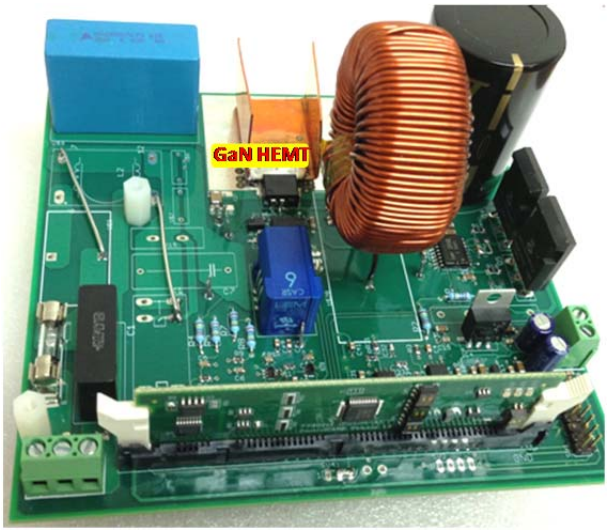

Fig.5 Photo of the prototype GaN totem pole PFC. The GaN HEMT pair is mounted on top and bottom of the PCB with a vertical alignment to minimize between them.

& S_2) are 600V super junction MOSFETs with 0.1 ohm on resistance. The inductor is made of a MPP core with inductance of 1.3 mH and a dc resistance 88 mohm, designed to operate at 50 kHz. D-tab and source-tab surface-mount GaN HEMT packages are used with one mounted on the top and another on the bottom side for the least electrical lengths between these fast switches, hence minimizing power loop inductances. A simple 0.5-A rated high/low side driver IC with 0/10 V as on/off states directly drives each GaN HEMT. A low-cost fixed-point 60 MHz DSP controller TMS320F28027DSP handles the control algorithm in this 1st version of prototype. The voltage and current loop control is similar to conventional boost PFC converter. The feedback signals are dc output voltage (V_O), ac input potentials (V_{ACP} and V_{ACN}) and inductor current (I_L). The input voltage polarity and RMS value are determined from V_{ACP} and V_{ACN}. The outer voltage loop output multiplied by $|V_{AC}|$ gives sinusoidal current reference. The current loop gives the proper duty-ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q_1 & Q_2. A soft-start sequence with a duty ratio ramps is employed for a short-period at each ac zero-crossing for better stability. Performance as a function of output power measured with a Yokogawa WT1800 power analyzer at 230 Vac input and 400 Vdc output is shown in Fig. 6. A peak efficiency of 99.0% is achieved at 400 W while the overall efficiency is >98.6% from 180W to 1kW. This outstanding performance from a simple topology is attributed to unconventional features of the new wide band-gap GaN power devices.

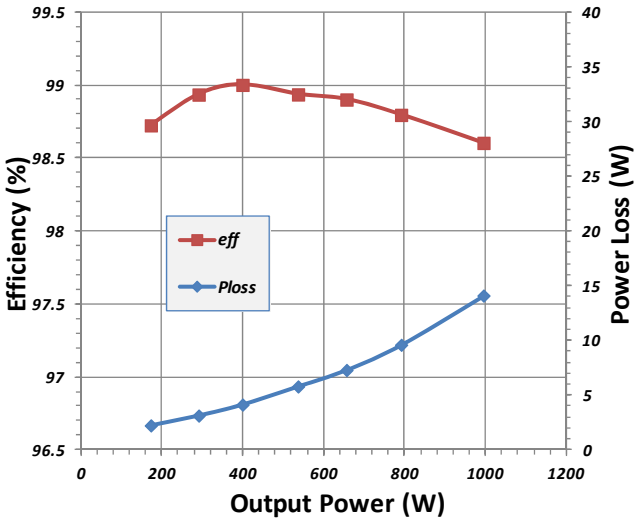

Fig.6 Measure efficiency performance of the GaN totem pole PFC with no diode drop in the current loop.

[CONCLUSION] The 1st generation GaN-on-Si high-voltage HEMT switch offers simultaneously low resistance and low stored charge, which successfully revived the long-abandoned hard-switched totem pole circuit. This elegant PFC consists the least number of fast power devices and features the least resistance current paths without a diode drop, achieving state-of-the-art conversion efficiency. With further circuit discoveries and innovations, the power electronics industry can benefit tremendously from the rise of GaN power devices.

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