Application Note:

TDPS250E2D2 All-in-One Power Supply Evaluation Board

1. Introduction

Transphorm has designed a complete 250 W power supply evaluation board specifically to meet the requirements for an all-in-one computer. The Power Supply combines a PFC input stage with an LLC DC-DC converter, using ON Semiconductor control ICs (NCP4810, NCP1654, NCP1397, NCP432) together with three Transphorm 600 V GaN high electron mobility transistors (HEMTs).

The compact-size board showcases GaN devices’ advantage in delivering both small size and high efficiency not possible with existing silicon solutions. It is designed to switch at 200 kHz in order to shrink the size and maintain high efficiency. With universal AC input, the All-in-One Power Supply Evaluation Board can deliver up to 20 A from the 12 V output with a peak efficiency of 95.4% from a 230 V ac line. The evaluation board is shown in Fig. 1.

Fig. 1. All-in-One Power Supply Evaluation Board
2. **TDPS250E2D2 Input/output Specifications:**

- Universal AC Input: 90-265Vac;
- Output: 12Vdc at 20A;
- PFC PWM Frequency: 200kHz;
- LLC Switching Frequency: 170kHz to 250 kHz ;

3. **Circuit Description for the All-in-One Power Supply**

Figure 2 illustrates the topology of the power supply. Three basic functions are shown: an input EMI filter, a boost-mode PFC circuit, and an LLC DC-DC converter. Not shown is a 12V DC regulator which provides power to the PFC and LLC controllers. The link between the PFC and LLC is a 390V DC voltage, identifiable in the schematic as the voltage across capacitor C1.

Figure 2: Simplified schematic for the complete power supply

The detailed schematic is included in pdf form with the kit documentation. The bill of materials is provided in Table I.

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While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the Transphorm GaN HEMT will switch at dV/dt of 100V/ns or higher. At this level of operation, even the layout becomes a significant contributor to performance. Figure 3 shows the layout of the layers in the evaluation board. The recommended layout minimizes the gate drive loop for each HEMT; it also keeps the traces between the switching nodes very short, with the shortest practical return trace to power ground. As the power ground plane provides a large cross sectional area to achieve an even ground potential throughout the circuit. Note that Transphorm GaN HEMTs in TO220 packages have a pin configuration of G-S-D, as opposed to the traditional MOSFET configuration of G-D-S. Placement of the source pin in the center reduces coupling between the input and output loops.

(a) Top layer
(b) Bottom layer

(c) Connections

Figure 3. PCB layers. Size: 5.84 inch × 2.55 inch (148mm x 64.8mm)
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<td>Common Mode Chk, 9mH, 1.9A, 22x15(mm)</td>
<td>4</td>
<td>MPS Inc.</td>
<td>P1131</td>
</tr>
<tr>
<td>81</td>
<td>L1, L2</td>
<td>Common Mode Chk, 9mH, 1.9A, 22x15(mm)</td>
<td>2</td>
<td>MPS Inc.</td>
<td>P5094</td>
</tr>
<tr>
<td>82</td>
<td>L4</td>
<td>Ind., 1mH, 70mA, 1210</td>
<td>1</td>
<td>Wurth Elek.</td>
<td>744045102</td>
</tr>
<tr>
<td>83</td>
<td>L5</td>
<td>Ind., 1mH, 0.235A, 7.0x7.6(mm)</td>
<td>1</td>
<td>Cooper Buss.</td>
<td>DRA73-102-R</td>
</tr>
<tr>
<td>84</td>
<td>LF</td>
<td>Ind., 480µH, 200kHz, CCC019</td>
<td>1</td>
<td>Precision</td>
<td>019-8202-00R</td>
</tr>
<tr>
<td>85</td>
<td>J1</td>
<td>CONN., 300V, 10A, 3Pin_3.5mm</td>
<td>1</td>
<td>Wurth Elek.</td>
<td>691214110003</td>
</tr>
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</table>
**4 Circuit Descriptions for the PFC AC-DC Converter**

![Generic NCP1654 Application Schematic](image)

*Shaded items are not installed.*

---

**Rev 1.4**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Component</th>
<th>Manufacturer / Part Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>2</td>
<td>J2, J3</td>
</tr>
<tr>
<td>87</td>
<td>2</td>
<td>HS2, HS3</td>
</tr>
<tr>
<td>88</td>
<td>1</td>
<td>PS1</td>
</tr>
<tr>
<td>89</td>
<td>1</td>
<td>MOV1</td>
</tr>
<tr>
<td>90</td>
<td>1</td>
<td>U2</td>
</tr>
<tr>
<td>91</td>
<td>1</td>
<td>U1</td>
</tr>
<tr>
<td>92</td>
<td>2</td>
<td>U3, U4</td>
</tr>
<tr>
<td>93</td>
<td>1</td>
<td>U5</td>
</tr>
<tr>
<td>94</td>
<td>1</td>
<td>U6</td>
</tr>
<tr>
<td>95</td>
<td>1</td>
<td>U7</td>
</tr>
<tr>
<td>96</td>
<td>1</td>
<td>F1</td>
</tr>
<tr>
<td>97</td>
<td>2</td>
<td>Q4, Q5</td>
</tr>
<tr>
<td>98</td>
<td>1</td>
<td>Transformer</td>
</tr>
<tr>
<td>99</td>
<td>3</td>
<td>FB1, FB2, FB3</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
<td>REC</td>
</tr>
<tr>
<td>101</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>102</td>
<td>1</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

*Figure 4 Generic NCP1654 Application Schematic*
Please refer to the datasheet of NCP1654 and application note AND8324-D from On Semiconductor Inc. in [1, 2]. Figure 4 shows a generic NCP1654 application schematic. The parameters of PFC controller and inductor are showed in Table II and III respectively.

### Table II Parameters of PFC controller

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Val</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{ac}</td>
<td>(Hz)</td>
<td>60</td>
<td>Ac line frequency</td>
</tr>
<tr>
<td>V_{acLL}</td>
<td>(V)</td>
<td>90</td>
<td>Ac line rms lowest level (generally 85 V or 90 V in wide mains applications)</td>
</tr>
<tr>
<td>V_{acHL}</td>
<td>(V)</td>
<td>265</td>
<td>Ac line rms highest level (generally 265 V in wide or European mains applications)</td>
</tr>
<tr>
<td>V_{ac,on}</td>
<td>(V)</td>
<td>75</td>
<td>Ac line rms voltage to start up (generally 75 Vac in wide mains applications)</td>
</tr>
<tr>
<td>V_{out}</td>
<td>(V)</td>
<td>385</td>
<td>Wished regulation level for the output voltage (generally 390 V or 400 V in wide mains apps)</td>
</tr>
<tr>
<td>V_{out,ll}</td>
<td>(V)</td>
<td>385</td>
<td>Minimum Output Voltage you can accept in normal operation - Use V_{out,ll}=V_{out} as a default value if you don't know</td>
</tr>
<tr>
<td>eff</td>
<td>(%)</td>
<td>95</td>
<td>Expected efficiency at low line, full load</td>
</tr>
<tr>
<td>P_{out}</td>
<td>(W)</td>
<td>216</td>
<td>Maximum output power</td>
</tr>
<tr>
<td>ΔI_{pk-pk}</td>
<td>(%)</td>
<td>30</td>
<td>Targeted peak to peak ripple of the coil current at low line and full load</td>
</tr>
<tr>
<td>R_{ds,ON}</td>
<td>(Ω)</td>
<td>0.29</td>
<td>MOSFET on-time resistance @ 25 °C</td>
</tr>
<tr>
<td>T_{hold-up}</td>
<td>(ms)</td>
<td>20</td>
<td>Hold-up time. Put 0 if no hold-up time is specified or if you don't know.</td>
</tr>
<tr>
<td>(V_{out})_{min}</td>
<td>(V)</td>
<td>310</td>
<td>Minimum output Voltage you can accept at the end of the hold-up time.</td>
</tr>
<tr>
<td>%DV_{pk-pk}</td>
<td>(%)</td>
<td>3</td>
<td>Peak to peak low frequency ripple that is acceptable across the bulk capacitor as a percentage of the regulation output voltage (&quot;V_{out}&quot;).</td>
</tr>
</tbody>
</table>

### Bulk Capacitor and Coil specification

| C_{bulk cal.} | (µF)  | 166 | Minimum C_{bulk} capacitance meeting the low frequency ripple and hold-up time constraints (*) |
|               |       |     | Choose higher standard value                                                  |
| C_{bulk Selected} | (µF) | 240 |                                    |
| ESR of C_{bulk} | (mΩ) | 150 | The ESR of C_{bulk}                                                          |
| L_{calc}      | (µH) | 397 | Proposed coil inductance                                                     |
| L Selected    | (µH) | 480 | Your inductance choice                                                       |
| (I_{coil})_{max} | (A) | 4.02 | Max peak coil current resulting from your inductance choice                   |
| (I_{coil})_{rms}  | (A)  | 2.53 | Maximum rms coil current                                                     |

### Conduction Losses

| Input Bridge | (W)  | 4.5 | Assuming the forward voltage of each diode is 1 V |
|             |      |     |                                                 |
| MOSFET      | (W)  | 2.9 | Assuming that R_{ds,ON} doubles at the highest junction temperature of your application |
Diode (W) 0.6 Assuming that RdsON doubles at the highest junction temperature of your application Assuming that the diode forward voltage is 1 V.

**Feed-back Arrangement**

| R_fbL (kΩ) | 23.2 | Choose a standard value |
| R_fbU1+R_fbU2 (kΩ) | 3,550 | (RfbU1+RfbU2) calculated based on RfbL and Vout. |
| C_fb (pF) | 100 |

**Input Voltage Sensing**

Choose high accuracy resistors for RboU1, RboU2 and RboL

| R_boL (kΩ) | 24.7 | Choose a standard value < 140 kΩ |
| R_boU1 + R_boU2 (kΩ) | 2,007 | (RboU1+RboU2) calculated based on RboL and Vac,on. |
| Cbo cal. (µF) | 1.69 | Cbo calculated based on RboL and line frequency |
| Cbo Selected (µF) | 2.20 | Choose the closest standard value. |
| V_ac,off cal. (V) | 64.5 | The calculated PFC brown out off threshold of AC input |

**Current Sense Network**

| Rsense cal. (Ω) | 0.17 | Value that makes the Rsense dissipation = ( 0.5% * Pout) |
| Rsense selected (Ω) | 0.06 | Your “Rsense” choice |
| P_Rsense (Ω) | 0.4 | Losses resulting from your Rsense choice |
| Rs cal. (kΩ) | 1.3 | Value resulting from your Rsense choice |
| Rs selected (kΩ) | 3.3 | Choose higher standard value |
| R_m (kΩ) | 110 | Value resulting from your Rsense choice |
| C_m (nF) | 2.2 | Value resulting from your Rm choice |

**Compensation Arrangement**

| F_z Hz | 20 | The wished cross over frequency at high line. |
| C_z cal. (µF) | 2.0 | The calculated Cz based on (G0)dB and fc. |
| C_z (µF) | 2.2 | Choose closest standard value |
| R_z cal. (kΩ) | 25 | The calculated Rz based on fz1. |
| R_z (kΩ) | 11 | Choose closest standard value |
| C_p cal. (nF) | 1.5 | The calculated Cp based on fp1 |

---

**Table III Parameters of PFC inductor**

<table>
<thead>
<tr>
<th>Items</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>480µH</td>
<td>~25% ΔIpk pk</td>
</tr>
<tr>
<td>Core Type</td>
<td>CC30/19</td>
<td>Height &lt; 20mm</td>
</tr>
<tr>
<td>Core Material</td>
<td>A-Core JPP-95</td>
<td>Similar to 3C95</td>
</tr>
<tr>
<td>Wire</td>
<td>40/38 Litz Wire</td>
<td>~0.11 Ω DCR</td>
</tr>
<tr>
<td>Winding Turns</td>
<td>38</td>
<td>&lt;10pF winding capacitance</td>
</tr>
<tr>
<td>Air Gap</td>
<td>~0.42 mm</td>
<td>Not considered fringing effect</td>
</tr>
</tbody>
</table>
5 Circuit Descriptions for the LLC DC-DC Converter

Figure 4 illustrates the topology of the LLC DC-DC converter portion of the evaluation board, which is based on the NCP1397 and NCP4304 controllers. The series capacitor forms the series-parallel resonant tank with leakage and magnetic inductances in the primary side of the transformer. From this configuration, the resonant tank and the load on the secondary side, act as a voltage divider. By changing the frequency of input voltage, the impedance of resonant tank will change; this impedance will divide the input voltage with load. The primary-side switches, Q1 and Q2, are the GaN HEMTs. Transistors SD1 and SD2 on the secondary side are synchronous rectifiers to improve the performance and efficiency. As may be seen in Fig. 4, there is no need for special gate drivers for the GaN HEMTs. Further information and discussion on the fundamental circuit schematics and the characteristics of LLC DC-DC converters are provided in [3]-[5].

![Circuit topology for LLC DC-DC converter using silicon MOSFETs for line rectification](image)

Fig 4. Circuit topology for LLC DC-DC converter using silicon MOSFETs for line rectification

Although the LLC is a resonant topology, characterized by soft switching, hard switching does nevertheless occur during start up. During this phase, the large reverse recovery charge (Qrr) of typical silicon MOSFETs causes problematic overshoot, ringing, and loss. Transphorm’s
TPH3002PS 1st-generation GaN power devices show a low on-resistance of 0.29 ohm typical and are capable of reverse conduction during dead time with a low Qrr of 29nC, more than 20 times lower than state-of-the-art Si counterpart as seen in Figure 5. These features can remarkably improve the performance and efficiency of hard-switch circuits, and are also important for hard starting in resonant circuits such as the LLC topology.

Fig.5 Reverse recovery charge test result for a Si MOSFET and a GaN HEMT with similar on resistance, showing a 20x reduction of Qrr for GaN.

Table IV gives a comparison of CoolMOS and GaN HEMT. The low Qrr will help reducing excessive spikes during start-up process in a LLC dc-dc converter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TPH3002PS</th>
<th>IPP60R380C6</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID</td>
<td>9A (continuous)</td>
<td>10.6A (for D=0.75)</td>
</tr>
<tr>
<td>Ron</td>
<td>290mΩ</td>
<td>340mΩ</td>
</tr>
<tr>
<td>Qg</td>
<td>6.2nC</td>
<td>32nC</td>
</tr>
<tr>
<td>Eoss(400V)</td>
<td>3.1µJ</td>
<td>2.8µJ</td>
</tr>
<tr>
<td>Qrr</td>
<td>29nC</td>
<td>3.3µC</td>
</tr>
</tbody>
</table>

Startup sequence:
1) Connect a load; The load should be resistive, and maximum of 240watt at 12Vdc;
2) Connect an AC power source, set to the desired voltage higher than 90V.
3) Place a cooling fan facing the GaN HEMTs heat sinks of PFC and LLC (provide a minimum of 30 CFM air flow);
4) Turn on the cooling fan if output power is higher than 150W;

Probing: In order to minimize additional inductance during measurement, the tip and the ground of the probe should be directly attached to the sensing points to minimize the sensing loop; while the typical long ground lead should be avoided since it will form a sensing loop and could pick up the noise. An example of low inductance probing is shown in Fig 6. The differential probes are not recommended for the GaN signal measurement.

![Fig. 6. Low-inductance probing of fast, high-voltage signals](image1)

Performance: Efficiency and Power Factor have been measured at low line (115Vac) and high line (230Vac) input for a range of loads on the 12Vdc output using the WT1800 precision power analyzer by Yokogawa. The results are shown in figure 7-9 for the complete power supply and
for the individual LLC circuits. The mid-load efficiency is more than 94% at low line and about 95.4% at high line, which is noticeably better than commercial boards with Si switches.

Figure 7. Efficiency for the power supply at 115V and 230V input
Figure 8. Power Factor vs. Output Power at 115V and 230V input

Figure 9. The efficiency result for the LLC DC/DC Converter circuit at 390Vdc input to 12Vdc output
Conducted emissions have also been measured for this board using a LIN-115A LISN by Com-Power. The results compared to EN55022B limits are shown in figure 10.

Standby power consumption is not optimized in this design for showing the superior performance over Si-based devices. Current Controlled Frequency Foldback (CCFF) and burst mode methods can be applied for very low power loss requirement at zero and light load using corresponding controllers and circuits.

**WARNING:** There are no specific current or voltage protection on this board; users need to follow the test procedure and operation limits carefully.

**REFERENCES:**


