1200V GaN Switches on Sapphire Substrate

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***Abstract*—We present results on 1200V GaN switches made with HEMTs on sapphire substrates. These are fast-switching, low loss devices extending the high performance of GaN switches to higher voltage levels. The insulating nature of sapphire substrates can help to extend the rated voltage of GaN HEMTs to 1200V and beyond, while simultaneously using a much thinner buffer layer compared to GaN-on-Si for similar voltages. Using a 70 mΩ GaN-on-sapphire 2-chip normally-off GaN FET in TO-247 package, we obtained >99% efficiency for a 900:450V buck converter operating at 50kHz. The GaN die has $R_{ON,sp}$ of 6.1mΩ.cm^2 and the device shows excellent switching FOMs with $R_{ON}.Q_G$ = 0.9 Ω.nC, and $R_{ON}.Q_{RR}$ = 11 Ω.nC. The sapphire substrate is thinned to below 200µm to give a thermal resistance comparable to that of packaged GaN-on-Si switches. These results indicate that a correctly engineered GaN-on-sapphire technology can be a very competitive platform for the 1200V power device market.**

Keywords—GaN-on-sapphire, GaN-on-silicon, GaN-on-Si, 1200 V, low-loss, high-efficiency, switching FOM

I. Introduction

GaN power switches have enabled higher efficiency and low system cost for power conversion applications due to the fast-switching and low losses in the switch [1][2]. State-of-the-art commercial GaN switches predominantly use silicon substrate and are fabricated in a GaN HEMT layer separated by a semi-insulating buffer from the substrate. 650V GaN-on-Si switches have achieved automotive qualification [3] and significant market acceptance [4] due to their superior performance compared to switches made with silicon or silicon carbide [5] at lower cost. 900V GaN-on-Si switches have also been released using lateral HEMT technology [6].

1200V GaN switches can enable similar performance improvements for applications such as EV drives, EV charging, PV inverters, and general 3-phase industrial applications [7]. 1200V rated devices on a GaN-on-Si platform would require use of very thick 10-12µm buffer layers, which adds significant cost and processing challenges [8]. GaN-on-engineered substrates [9], and GaN-on-GaN [10][11] research approaches have also been demonstrated but both require expensive >10µm epitaxial growth on expensive substrates. The insulating nature of sapphire reduces electric-fields in the semi-insulating buffer layers and enables 1200V devices with substantially thinner buffer layers than the 10-12µm expected for GaN-on-Si. This in turn reduces MOCVD growth cost, reduces stress in the underlying substrate and as a result can enable future scaling of substrate size to 200-mm or more for high throughput and lower manufacturing cost. 150-mm sapphire is widely used in the GaN LED industry today and is low cost (< $100) and recently 200-mm sapphire has also become commercially available [12]. Backend and assembly of sapphire-based GaN devices are also well established and commercially available services. This makes sapphire very well suited as a substrate for GaN power switches.

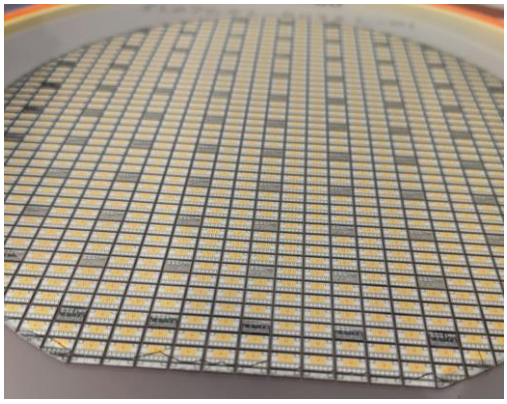

Fig. 1. 150-mm GaN-on-sapphire wafer with 1200V switches; thinned, diced and ready for packaging.

In this paper, we demonstrate the viability of correctly engineered GaN-on-sapphire technology for 1200V power switches, and share comprehensive characterization of the devices including leakage, breakdown, dispersion, thermal resistance, inductive switching, and converter efficiency. We show how such a GaN-on-sapphire technology can be a strong enabler for voltage scaling of GaN HEMTs and high performance, manufacturable, low cost switches for 1200V and beyond.

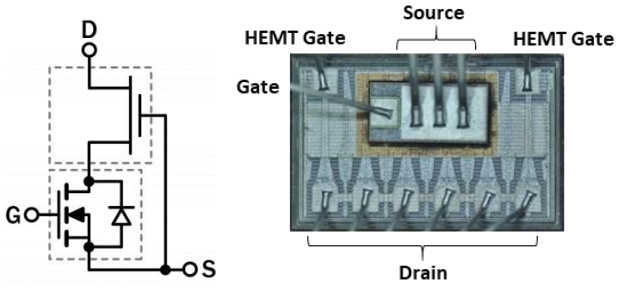

Fig. 2 (a) Circuit schematic of cascode switch configuration and (b) microscope image of the two-chip normally-off 1200V switch showing the die-on-die design and sapphire substrate directly bonded to the TO-247 package leadframe.

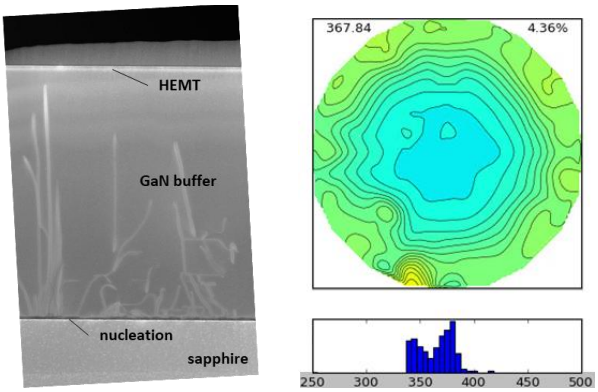

Fig. 3 (a) TEM cross-section of the GaN-on-sapphire epitaxy for 1200V switches, with low dislocation density near the active layers and (b) wafer level contactless R_{sh} showing median R_{sh} of 368 Ω/sq. and excellent R_{sh} uniformity of 4.4% over a 150-mm wafer (blue is lower R_{sh}).

II. Device Design and Characteristics

A. Device design

The semi-insulating GaN buffer (Fig. 3a) was hetero-epitaxially grown on a 150-mm sapphire substrate using proprietary growth methodologies. The XRD FWHM values are excellent at 0.09° in 002 and 0.17° in 201 directions. This indicates very good material quality. Wafer level contactless sheet resistance measurement shows excellent uniformity of 4.36% (Fig. 3b). The 1200V devices were fabricated in a CMOS compatible wafer-fab line using process modules very similar to the established GaN-on-Si line, with sapphire thinning and dicing done on commercial tools (Fig. 1). A proprietary insulated field-plate architecture was used for electric-field management. This first generation device has a 16.59mm^2 die area and is designed to target a normally-off product with datasheet R_{ON} of 70mΩ. A 30V Si MOSFET is die attached on top of the GaN HEMT to realize the robust normally-off switch (Fig. 2). The Si MOSFET has a gate voltage rating of +/- 20V and Vth ~ 4V. This allows the device to be driven using standard gate drivers with a robust input interface.

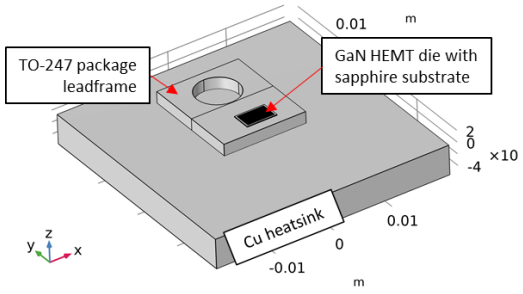

Fig. 6. 3D thermal model of GaN power HEMT in TO-247 package. Model estimate of Rth is in good agreement with measured Rth of 0.78°C/W

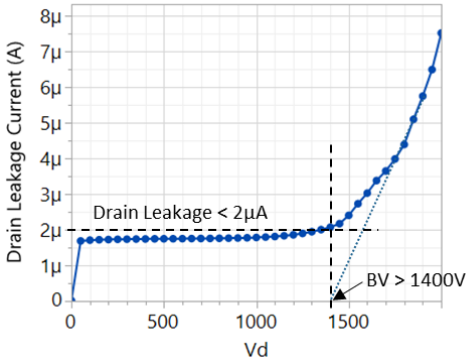

Fig 4. Off-state I-V curve, showing low leakage of < 2μA at 1200V and a breakdown voltage of more than 1400V.

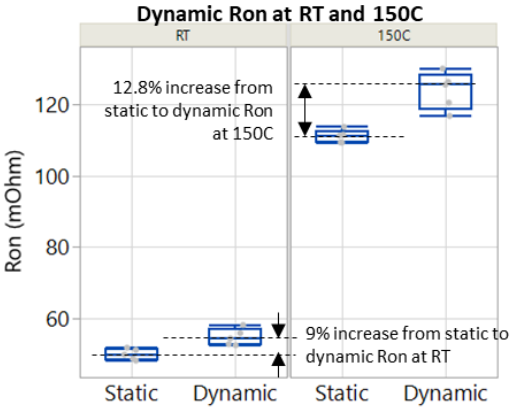

Fig. 5. Less than 10% increase in R_{ON} from static to dynamic conditions at RT and less than 13% at 150°C.

B. Device Characteristics

The device leakage stays below 2μA upto 1200V and device breakdown voltage is greater than 1400V (hard-breakdown voltage is even higher >2kV) giving an adequate voltage margin (Fig. 4). GaN-on-sapphire, due to its insulating nature, keeps vertical buffer fields minimal and enables large lateral blocking voltages with buffer thickness much less than that for GaN-on-Si. $R_{ON,sp}$ of this first generation GaN HEMT die is 6.1mΩ.cm^2.

To test the dynamic trapping behavior, R_{ON} of the devices was measured 1 μs after turn-ON following application of a blocking of 960V for 20ms in the OFF state (Fig. 5). The devices showed 9% R_{ON} increase compared to the static R_{ON}. R_{ON} increase under dynamic conditions at 150°C was 12.8% thus validating that the device design and epitaxial material quality are suitable for 1200 V switches in application (Fig. 5).

Junction-case thermal resistance ($R_{th,j-c}$) is a key parameter for high-power devices. First, we modeled the thermal resistance of a die in a TO-247 package (Fig. 6) and identified that 100μm thick sapphire substrate can match the thermal resistance of a GaN-on-Si device. Based on this model, and as a first conservative step, the fabricated GaN-on-sapphire wafers were thinned down to 200μm and singulated. Thermal resistance measured on thinned, singulated, and packaged

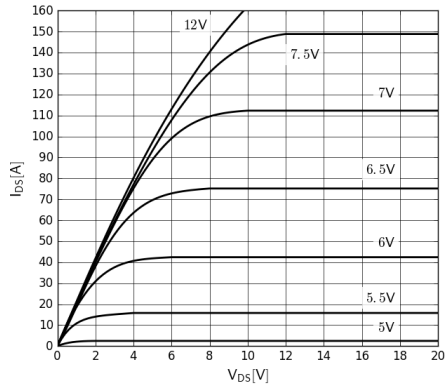

Fig. 7. Well behaved output characteristics showing very high pulsed current > 160A resulting from substrate thinning and thermal resistance of 0.78°C/W.

devices is 0.78°C/W and in good agreement with the predictions of the model. Substrate thinning to 100µm (the target thickness) is well within the range offered by commercial vendors. Output characteristics of the device show high pulsed current > 160A (Fig. 7). This again shows that the device has good thermal characteristics and can achieve high current levels.

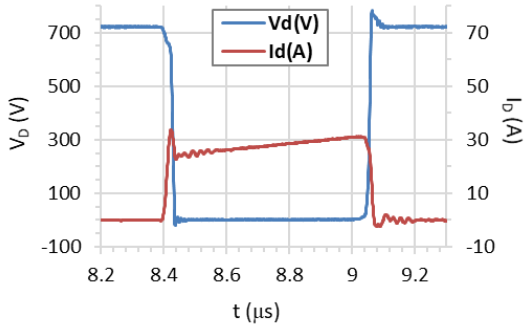

Fig. 9. Half-bridge inductive switching waveform at 720V/28A showing well behaved waveforms with tr ~ 14ns and tf ~ 13ns.

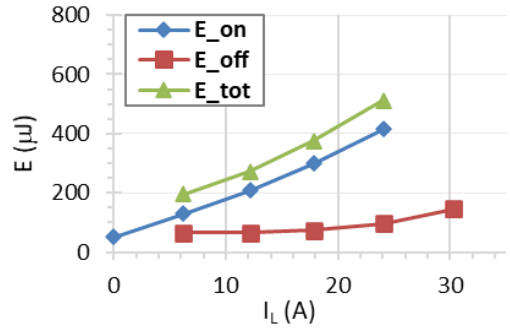

Fig. 10. E_{on}, E_{off}, and E_{tot} extracted from 720V half-bridge inductive switching waveforms for 1200V GaN-on-sapphire device in TO-247 package.

Switching FOMs	SoA SiC	1200V GaN
$R_{ON}Q_G$	4.3 Ω.nC	0.9 Ω.nC
$R_{ON}Q_{RR}$	19.2 Ω.nC	11 Ω.nC

Fig. 8. 1200V GaN switching FOMs are superior to state-of-the-art 1200V SiC MOSFETs.

III. Figure-of-Merits and Switching Performance

A. *Device FOMs and comparison to state-of-the-art*

Q_G, Q_{OSS}, and Q_{RR} are key metrics that determines losses in hard-switched applications. Q_G is primarily determined by the Si MOSFET and is 15 nC for the MOSFET used here. Q_{OSS} of the device is 185 nC at 800 V. Q_{RR} is nominally the same as Q_{OSS} (185nC at 800V) since the stored minority charge in the device is negligible. The switching FOMs for the 1200V GaN-on-sapphire device are: $R_{ON}.Q_G$ = 0.9 Ω.nC, $R_{ON}.Q_{OSS}$ = 11 Ω.nC, and $R_{ON}.Q_{RR}$ = 11 Ω.nC. The switching FOMs of the 1200V GaN-on-sapphire device are excellent and the $R_{ON}.Q_G$ and $R_{ON}.Q_{RR}$ are better than state-of-the-art SiC devices (Fig. 8) [13]. Both wide-bandgap technologies have significantly better switching FOMs compared to silicon IGBTs and should perform much better in power switching applications.

B. *Switching and converter efficiency*

Inductive switching testing in a half-bridge circuit was performed at 720V/28A to capture the turn-on and turn-off transients (Fig. 9). Using an R_G = 47Ω, the waveforms are well behaved and show fast rise and fall times t_r ~ 14ns and t_f ~ 13ns. The total losses increase at higher current levels as expected due to higher turn-on loss with the total switching losses being 510µJ per switching cycle at 720V/24A (Fig. 10).

A 900:450V buck converter was built to test the efficiency of the devices at 50kHz and 100kHz (Fig. 11). Both high and low-side devices were GaN-on-sapphire 1200V/70mΩ devices. The circuit was operated in synchronous mode with dead time set appropriately to prevent shoot-through. During the turn-on transient, the inductor current is transferred from the reverse-

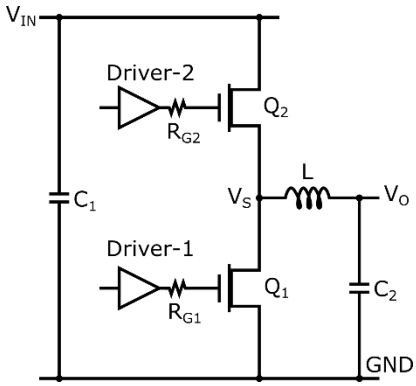

Fig. 11. Schematic circuit of 900:450V synchronous buck converter using two 1200V GaN switches (Q1/Q2) operated in hard-switched mode.

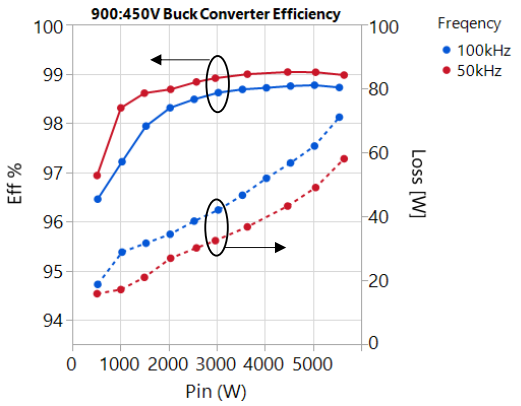

Fig. 12. Efficiency and power loss of a 900:450V buck converter operated at 50kHz and 100kHz in synchronous hard-switched mode. Peak efficiency is >99% at 50kHz and 98.7% at 100kHz.

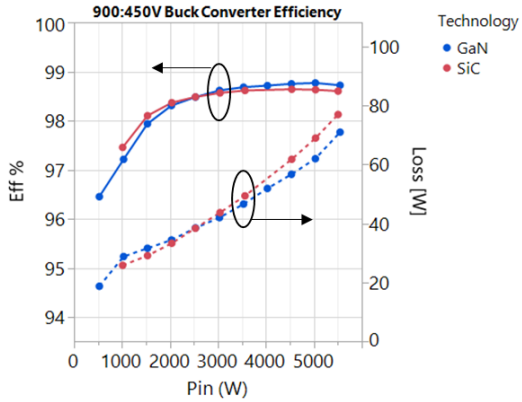

Fig. 13. Efficiency and power loss of a 900:450V buck converter operated at 100kHz in synchronous hard-switched mode. Peak efficiency of GaN is 98.76% vs 98.63% for SiC MOSFET.

conduction state of low-side device (Q1) to the high-side device (Q2). The Q_{OSS} and Q_{RR} of Q1 are also discharged through Q2 during this transition. Q2 therefore goes through a hard-switching event at every turn-on transition. The low Q_{OSS} and Q_{RR} of GaN-on-sapphire devices are key to achieving low switching loss. At a frequency of 100kHz, Q1 and Q2 are conducting for roughly 5µs each. 900:450V buck converter efficiency is > 99% at 50kHz and 98.7% at 100kHz (Fig. 12), which can be further optimized by reducing inductor losses. The low dynamic R_{ON} was key to attaining the low conduction loss required to achieve the measured high efficiency. Buck converter efficiency using GaN-on-sapphire devices is higher than state-of-the-art SiC MOSFETs (Fig. 13). This result clearly demonstrates the promise of GaN-on-sapphire as a high-performance and low-cost 1200V solution.

IV. Conclusion

GaN HEMTs on sapphire were designed and fabricated to extend the voltage range of lateral GaN FETs to 1200V. 1200V/70 mΩ GaN FETs were built using this GaN-on-sapphire technology and the performance was evaluated under various operating conditions. The devices demonstrated excellent leakage, dynamic R_{ON}, and switching FOMs. 900:450V buck converter efficiency was > 99% when operated at 50kHz. The GaN-on-sapphire converter efficiency was better than state-of-the-art SiC MOSFETs owing to the superior switching FOMs. This work supports the promise of correctly engineered GaN-on-sapphire as a high-performance and low-cost solution for power conversion applications that require 1200V blocking voltage.

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