A 650V/780A GaN Power HEMT Enabling 10kW-Class High-efficiency Power Conversion

Y.-F. Wu[1], C. Neufeld[1], S. Wienecke[1], B. Swenson[1], M. Kamiyama[2], T. Ogino[2], J. Ikeda[2], Y. Miyazaki[2], T. Hosoda[2], K. Imanishi[2], R.P. Smith[1], Y. Huang[1], J. Guerrero[1], S. Yea[1], R. Birkhahn[1], M. Moore[1], S. D. Chowdhury[1], and L. McCarthy[1]
[1]Transphorm Inc., 115 Castilian Drive, Goleta, CA 93117, USA, Email: ywu@transphormusa.com
[2]Transphorm Japan Inc., 3 Kogyodanchi, Monden-machi, Aizu-Wakamatsu, 965-8502, Japan

Abstract—A 650V-rated GaN-on-Si HEMT with a maximum current of 780A in a die size 33mm^2 was developed by effective scaling. Clever integration with a low-voltage Si MOSFET resulted in a cascode FET with a high threshold of 4V, stable dynamic on-resistance of ~14mΩ up to 750V and single-chip-like package simplicity. Using a simple gate drive of (0, 12)V and a low drive current below 0.7A, the co-pack device in a TO-247 package of high thermal capacity exhibited much faster switching transients and 2x lower switching losses than a competing SiC MOSFET. When implemented in a 240V:400V half-bridge synchronous boost converter, 12kW output power with >99% peak efficiency was achieved.

I. Introduction

Since the launch of the 1st 600V GaN-on-Si power device in 2013[1][2], GaN power electronics has been steadfastly accepted into the market[3]. However, current qualified 600V/650V GaN transistors are capable of only 2-5kW output power per device limited by the non-trivial current distribution in the horizontal structure and the restricted heat removal from the surface-mount packages chosen by the p-gate E-mode device structures with poor gate overvoltage tolerance. With a robust gate reliability, the cascode GaN FETs can use high-thermal-capability thru-hole packages therefore are more suited for higher power applications, but the 2-chip configuration adds complexity in packaging. This work describes a significant advance in device scaling and integration to obtain a 650V/14mΩ GaN power switch with a high threshold voltage, high pulse current and 1-chip-like packaging simplicity.

II. Device Design & Characteristics

The high-voltage GaN HEMT was built on a >5µm thick epi grown on a 6-in Si substrate. The gate length is 1µm with multiple field plates for electric field management. The device pitch is 24.5µm long with 2.5µm source/drain ohmic contacts, 19.5µm channel. The total gate periphery is 1039mm with 452 sub cells. The devices were fabricated in a CMOS compatible wafer process line with a 2–µm-thick Al on the ohmic area for enhanced conductivity, a 2nd 6-µm-thick Al metal as interconnect to carry the current in-and-out of each cell, and a 3rd 8-µm-thick Al metal to form the source and drain pads. The finished GaN die has a total dynamic resistance of ~10.5mΩ including ~8mΩ of the intrinsic HEMT and ~2.5mΩ from total metal interconnects. With a total die area of 33mm^2 including edge termination and dicing street, the GaN die specific on-resistance is 3.47mΩ-cm^2, close to that of 650V SiC MOSFETs[4] w/o the complexity of surface current routing. This favorable figure-of-merit and the low-cost potential of the GaN-on-Si make it a competitive technology.

This D-mode GaN HEMT die was specifically designed to mate with a E-mode 30V/1mΩ Si MOSFET on the source pad as shown in Fig.1, resulting in a normally-off cascode FET with only 3 sets of wire bonds similar to a single-chip FET. Unlike present E-mode GaN devices with a poor gate overvoltage margin therefore limited to surface-mount packages generally implemented for well below 2kW applications, the robust gate of our GaN FET allows the use of the TO-247 thru-hole package for several times higher heatsinking capability.

The final device is shown in Fig. 1(c) with G-S-D pin out and the metal pad as the common source for a natural signal flow to promote good input-output isolation. It has a reliable gate voltage rating of +/-20V and a high threshold (V_{TH}) of +4V at I_D=2mA. The gate charge (Q_G) is 68nC, about 36% of similarly-rated SiC MOSFETs[5]. The combination of a high V_{TH} and low Q_G makes the GaN FET the easiest to drive among competing devices with no need for spike clamping or negative V_G. The I-V characteristics are shown in Fig.2 exhibiting an on-resistance of <13mΩ (after including resistances of the low-voltage Si MOSFET, wire bonds and leads) and a very-high pulse current of 780A. This is excellent scaling, corresponding to 750mA per mm of gate periphery for such a large device. The off-state drain leakage was tested at room temperature (RT), 150°C and 175°C respectively as plotted in Fig. 3. The device exhibits a large voltage margin over the 650V rating, with a soft breakdown voltage of 1200V at RT and 1000V at 175°C at a drain leakage current of 0.6mA, or 0.56µA/mm.

An additional feature of the hybrid GaN FET is the reverse conduction capability in off-state with a low voltage drop of the Si MOSFET body diode and the open GaN HEMT channel. The dynamic reverse-recovery-charge (Q_{RR}) tested at 60A/400V is 430nC, the same as the output stored charge (Q_{OSS}) in off-state, indicating minimum internal minority charge in reverse conduction. This is due to the high-speed low-voltage Si MOSFET design and the absence of minority charge in the high-voltage GaN HEMT. Compared to the competing SiC MOSFET having a lower Q_{OSS} of 206nC but a Q_{RR}/Q_{OSS} ratio of 2-3 at high current and temperatures[5], the GaN FET should offer a broader efficiency curve over output power. Both GaN and SiC devices are superior to typical 650V Si MOSFETs having a Q_{RR}/Q_{OSS} ratio of 10-100, which is a key advantage of the wide-band-gap devices, enabling very-low losses in bridge converters that require reverse conduction to support the inductive free-wheeling current.

III. Switching Operation & Converter Performance

To evaluate charge trapping in the GaN HEMT channel over the whole voltage-temperature space, dynamic on-resistance as defined as the $R_{DS(ON)}$ value immediately (~1µs) after blocking high voltages was tested at room 25 °C (RT) and 150°C as shown in Fig.4. Each data point was taken after soaking at the stress voltage for 1 min. The device maintains a low on-resistance about ~14mΩ at RT, ~25mΩ at 150°C and ~28mΩ at 175°C respectively throughout the voltage range up to 750V, ensuring efficient current conduction in switching conditions even with voltage transients well above the 650V rating. The minor humps around 100V-200V are related to the electric field optimization for higher instead of lower voltages. The overall excellent dynamic $R_{DS(ON)}$ properties are a result of years of extended effort in electric field engineering and material growth optimization of the high-voltage GaN HEMT structure.

Inductive operation waveforms in a half-bridge (with a low-side & a high-side device: Q1 & Q2 as in Fig.7.) at 400V and 65A was investigated in Fig. 5 comparing to that of a 650V/15mΩ SiC MOSFETs[5] also in TO-247 packages. The gate drive was (0, 12)V with a R_G=15Ω (peak current ~0.7A) for the GaN FETs, which was enhanced to (-4, +15)V with a R_G=5Ω (peak current ~2.1A) for the SiC MOSFETs. Even with a much lower driving strength, the GaN devices deliver higher current and voltage switching speeds of 4kA/µs and 60kV/µs, about 2 times over that of the SiC. This is attributed to the fundamentally superior electron transport in GaN. Note that the turn-on process is a hard-switched event where the inductor current transitions from S-D in Q2 to D-S in Q1. Q1 must first take over the inductor current, then discharges the Q_{RR} of Q2 and brings down the drain voltage to enter full conduction. The inductor current, Q_{RR} and switching time determine the turn-on loss. In the turn off process, Q1 switches from on to off and the body diode of Q2 offers the free-wheeling function for the inductor current to pass with no obstruction. Since there is no Q_{RR} dissipation, the inductor current and switching time determine the turn-off loss. Fig.6 plots the switching losses versus inductor current. With similarly low Q_{RR} as the SiC MOSFET, the higher speed of GaN translates to a reduction of switching losses by about 50% at high current levels.

Finally, the half-bridge circuits were configured into a 240V:400V boost converter with the simplified circuit diagram in Fig.7. The heatsinks for the low-side and high-side devices Q1 & Q2 have thermal resistances of 0.8 and 1.2°C/W respectively, where the difference reflects the consideration that Q1 consumes most of the switching losses. The main passive components include input/output film capacitors C1/C2 of 18/20µF with series resistances (ESR) about 2mΩ, and a 300uH boost inductor L with an ESR of 13.5mΩ. Each switching cycle includes two main states—State-1: Q1 is on and Q2 is off, inductor L absorbs the energy from the input source at V_{IN} and State-2: Q1 is off and Q2 reverse conducts, inductor energy releases to the output V_O. Conduction losses related to the current and $R_{DS(ON)}$ of Q1 and Q2 are the main power losses in these two statice states. The transition from State-1 to State-2 is a significant switching loss event shown in the "turn-off" waveforms in Fig.5. Immediately after this transition both transistors are still "off" per the gate control, hence it is called the "dead-time" state, which is set for 0.5µs in our converter, a small fraction of the total period. After the dead-time, it is now safe to turn on Q2 to bypass the diode drop for a reduced conduction loss. The next is a second dead-time state when Q2 is turned off and the current passes its body diode. The circuit is then ready for the transition from State-2 back to State-1 which is a major switching loss event as shown in the "turn-on" waveforms in Fig. 5 and described earlier.

The converter was tested at 70kHz with performance as a function of output power plotted in Fig.8. As expected from the well-behaved dynamic $R_{DS(ON)}$ and the outstanding switching speed, the GaN converter outperforms that of the SiC, delivering 12kW output power and a peak efficiency well above 99%. Considering the significant ESR of the inductor comparable to that the of the active devices among other losses, the GaN device efficiency is estimated close to 99% even at 12kW. Although with a higher junction-to-case thermal resistance of 0.4°C/W than the 0.35°C/W value for the SiC MOSFET, based on the measured case temperature and heatsink thermal resistance, the junction temperature of the Q1 GaN FET was estimated to be 139°C at 12kW output power, while that of the SiC MOSFET was already 166°C at 11kW and would exceed the 175°C rating at 12kW. This exemplifies the importance of electrical performance enabled by GaN.

IV. Conclusion

A large-periphery high-voltage GaN HEMT was engineered to expand the operation space of the horizontal device. This was cleverly integrated with a low-voltage Si MOSFET resulting in a GaN cascode FET with a robust gate tolerance +/-20V, a high 4V threshold voltage, 650V rating and 780A pulse current. It also demonstrated outstanding switching speed under a very-simple gate drive and superior converter efficiency up to 12kW without paralleling. This and the low-cost potential support a strong prospect of the GaN-on-Si FET for >10kW high power conversion applications.

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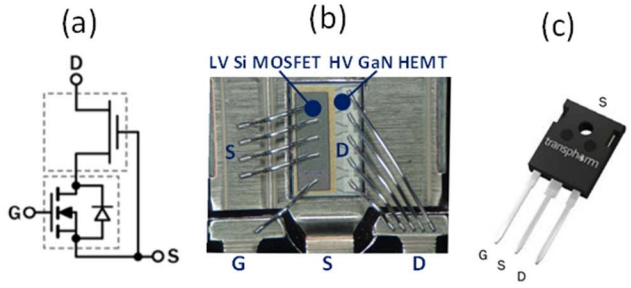

Fig. 1. The 2-chip normally-off cascode GaN FET. (a) Circuit representation. (b) Internal package configuration. (c) Finished device in TO-247 with G-S-D pin allocation and the metal pad as another S terminal.

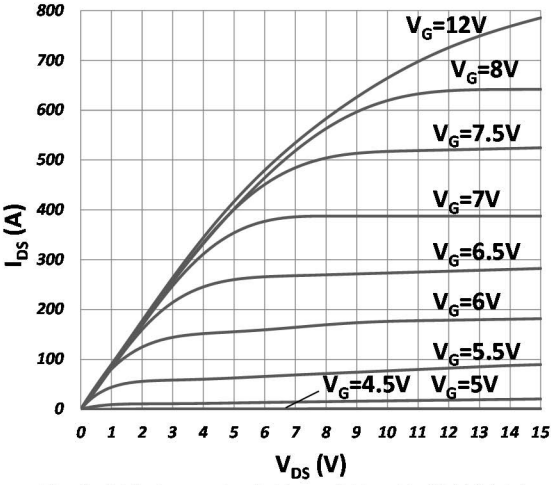

Fig.2. I-V characteristics of the GaN FET. The device has a Vth=4V at 2mA, on-resistance 13mΩ at V_G=12V, and max pulse current I_{DMAX}=780A.

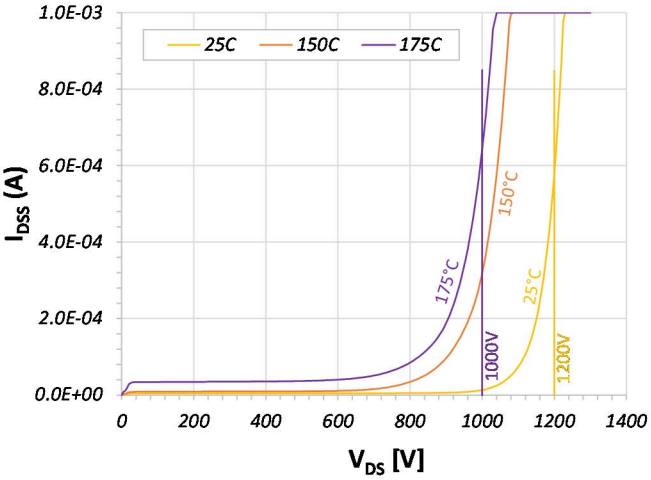

Fig. 3. Off-state breakdown characteristics (V_G=0) showing soft breakdown of 1200V at 25°C and 1000V at 175°C defined at I_D=0.6mA.

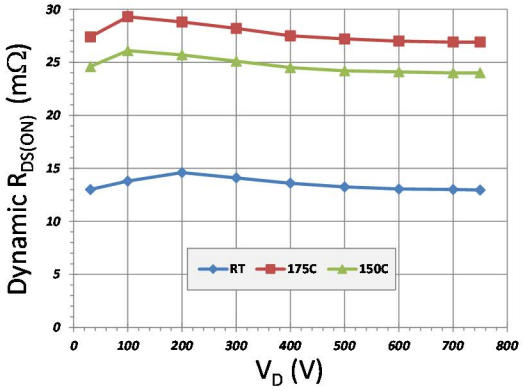

Fig. 4. Dynamic on-resistance vs. blocking voltage at 25°C, 150°C and 175°C.

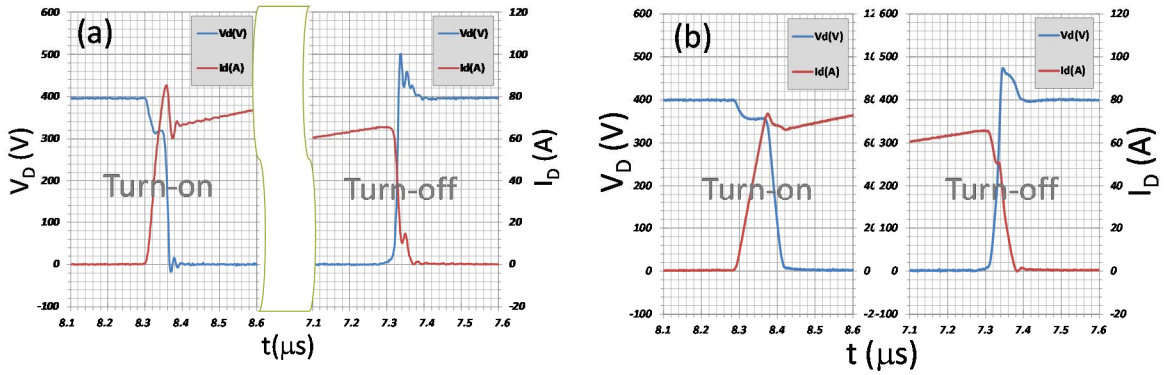

Fig. 5. Inductive switching waveforms at 400V/65A for (a) the GaN FET and (b) a SiC MOSFET (C3M0015065D).

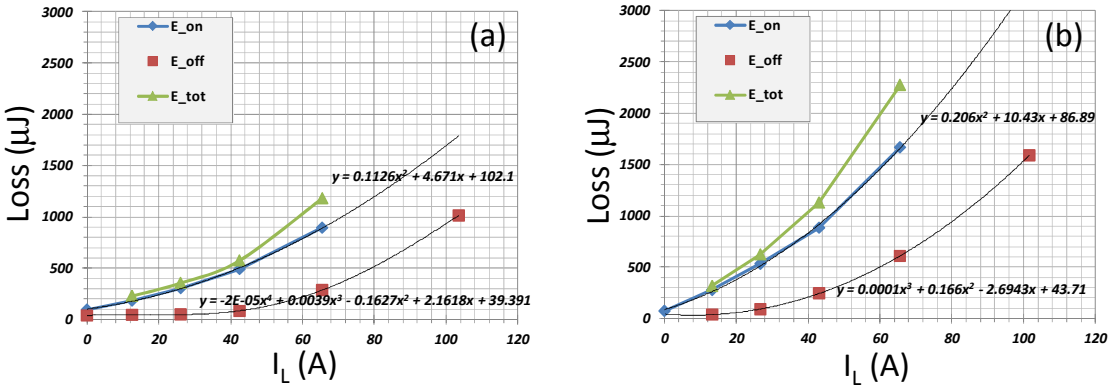

Fig. 6. Switching loss vs. current for (a) the GaN FET and (b) the SiC MOSFET. Gate drive conditions: (0, 12V), R_G=15Ω for GaN; (-4V, 15V), R_G=5Ω for SiC).

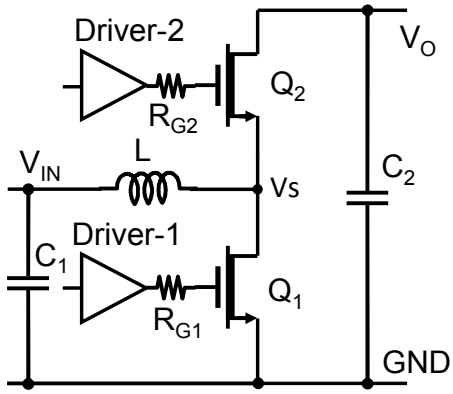

Fig. 7. Simplified schematic of the bridge boost converter for performance test of power devices.

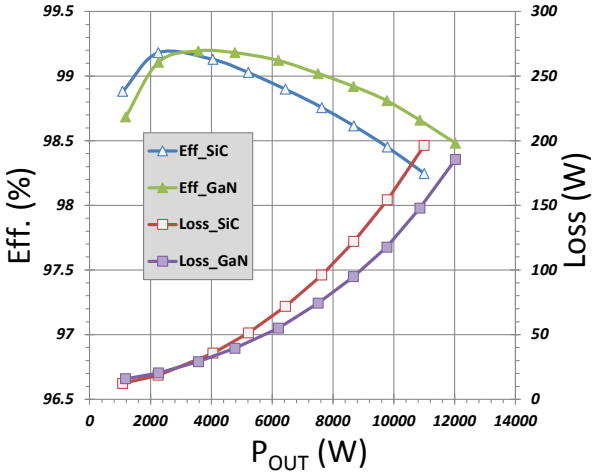

Fig. 8. Performance comparison of the 240V:400V half-bridge converter using the GaN FETs and the SiC MOSFETs at 70kHz.