Recommended External Circuitry for Transphorm GaN FETs

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Part I: Introduction

Transphorm GaN FETs provide significant advantages over silicon (Si) superjunction MOSFETs by offering lower gate charge ($Q_g$), faster switching speeds, and lower body-diode reverse recovery charge ($Q_{rr}$). GaN FETs exhibit in-circuit switching speeds much higher than that of the current Si technologies. The inherent rapid switching of GaN devices reduces current/voltage cross-over power losses, enabling high frequency operation while simultaneously achieving high efficiency.

However, the accompanying high $dI/dt$ transient during switching, combined with parasitic inductances, generates noise voltages in the circuit. This noise can interfere with the gate and the driver of the device, and, in the worst case, creates sustained oscillation that must be prevented for safe operation of the circuit. This application note provides guidance on how to eliminate oscillation and how to achieve high switching current with a controlled $dI/dt$.

Part II: Solutions to Suppress Oscillation

To avoid sustained oscillation, it is important to minimize noise generation, to minimize noise feedback, and to damp the ringing energy resulting from the high current/voltage transients. This can be achieved with the recommendations outlined below using a half-bridge switching circuit in Figure 1 as an example.

![Figure 1. a) Half-bridge switching circuit and b) Efficiency vs. output power](image)

1) **Optimize the PCB layout** to minimize external parasitic inductances and associated feedback. Use a large area ground plane for an overall low-noise base potential. Arrange the gate drive circuit on one side and the output circuit on the other side to minimize noise feedback from the output loop to the input loop. Place the driver circuit close to the gate of the device. Shorten the power loop by arranging the high-side and low-side devices close-by.

2) **Use a gate ferrite bead** [FB1 in Figure 1(a)] to prevent the high-frequency noise from entering the driver and logic circuits. This bead should be mounted close to the Gate lead of the device. NOTE: This is required even for single-ended non-half-bridge designs. The specification of the recommended gate ferrite beads are listed in Transphorm’s GaN FET datasheets and also summarized in Table 2. The TO247 package includes a built-in gate ferrite bead for our Gen III devices but has been moved to the outside for our latest Gen IV (G4) devices. Please refer to page three of the datasheet to verify its position.
3) **Use a DC-link RC snubber** \([R_{C\text{DCL}} \text{ in Figure 1(a)}]\). The DC rail or DC-link, when decoupled with a low-ESR fast capacitor, can be considered a high-Q C-L network at high frequencies (with "L" being the feed inductance of the DC bus). This can interact with the devices at voltage/current transients and lead to ringing. Adding an RC snubber across the DC-link close to the drain pin of the high-side device can effectively absorb the ringing energy, suppressing potential oscillation. This effect is shown in Figure 2 where the high-frequency ringing at 25 A turn-off is substantially damped with the \(R_{C\text{DCL}}\). Since this snubber is not inserted at the switching node, it does not add switching loss to the circuit. NOTE: This is recommended even for single-ended non-half-bridge designs. The practical values of the \(R_{C\text{DCL}}\) can be 2 sets of 6-10\(\Omega\)/0.5W SMD resistors in series with a 10nF/600-1000V ceramic SMD cap, or 1 set of 3-4\(\Omega\)/1W resistors in series with a 10-20nF/600-1000V cap if space is limited.

4) **Adding a switching-node RC snubber** \([R_{C\text{SN}} \text{ in Figure 1(a)}]\) can further reduce high-frequency ringing and help control di/dt transients at high operation currents. The effect of the \(R_{C\text{SN}}\) on switching waveform at a switching current >50 A is shown in Figure 3. Unlike the \(R_{C\text{DCL}}\), the capacitance of the \(R_{C\text{SN}}\) does increase switching loss. The recommended snubber parameters with little degradation in efficiency are given in the datasheet and are summarized in Table 2 for both single \(R_{G}\) and dual \(R_{G(ON)}/R_{G(OFF)}\) use.

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**Table 2**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single (R_{G}) Use</th>
<th>Dual (R_{G(ON)}/R_{G(OFF)}) Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{C\text{SN}}) (\Omega)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>(C_{C\text{SN}})</td>
<td>100pF</td>
<td>100pF</td>
</tr>
</tbody>
</table>

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Figure 2. Half-bridge inductive switching waveforms with decoupling capacitor only and with DC-link snubber \((R_{C\text{DCL}})\)
(Devices: TP65H050WS)

Figure 3. Effect of switching node snubber \(R_{C\text{SN}}\) on half-bridge inductive switching waveforms
(Devices: TP65H035WS).
Part III: The di/dt Limits of GaN Switching Devices & Solutions for High-current Operation

Transphorm GaN FETs are designed for the highest robustness and reliability within the technology boundaries today. These devices can operate to their full voltage rating and at extremely high di/dt levels in normal operation mode (forward conduction when current enters the Drain). However, when used as a free-wheeling device in reverse conduction mode (current enters the Source when the Gate is off), there are di/dt limits beyond which the performance can be negatively affected. Although these reverse conduction di/dt limits in the range of 1900~3500 A/µs (depending on device & stress duration) are much greater than that of typical superjunction devices at ~60 A/µs, care must be taken for best performance at high current levels since the di/dt value is a strong function of switching current.

It is important to note that this di/dt limit only applies to the device acting as a free-wheeling diode (FWD) and only applies to the duration when the FWD transitions from blocking voltage to reverse conducting current. Three cases are illustrated in Figure 4: the affected devices are the ones functioning as an FWD during dead-time when the inductor current commutates from the main switch to the reverse current of the FWD.

1) A boost converter that uses a SiC diode as the rectifier device – Not affected.
2) A synchronous boost that uses a GaN FET as the FWD – Q2 affected.
3) A synchronous buck that uses a GaN FET as the FWD – Q1 affected.

The maximum di/dt stress happens when the main switch [Q2 in Figure 4 (2) or Q2 in Figure 4 (3)] turns off and the inductor current redirects to the FWD instantly. The higher the turn-off current, the higher the reverse conduction di/dt. The reverse conduction di/dt limits (di/dt_{RM}) is listed in the datasheet (Table 1).
Table 1. TP65H035G4WS reverse diode conduction di/dt limits and associated max switching current when using the recommended Rs and RCSN.

Note that the reverse diode switching current limits were obtained with the recommended circuit parameters [Figure 1(a) and Table 2]. The gate resistor(s) are important to control the di/dt and the addition of a switching node snubber RCSN offers further improvements when operation current is high. The effect of RCSN is shown in Figure 1(b): a slight reduction in low-load efficiency, but a significant enhancement at high load. In applications with Rs is equal to or higher than the recommended value, the RCSN can be omitted. In all situations, care has to be taken to ensure junction temperature of the devices do not exceeding maximum rating.

Part IV: Additional Design Notes

1) Circuit and Layout Recommendations

- As GaN FETs switch extremely fast, we recommend using a driver(s) with sufficient Common Mode Transient Immunity (CMTI) so as not to cause disruption between the secondary and primary side of isolated drivers when in operation.
- When using the GaN FETs in a half bridge configuration, we recommend using an integrated half bridge gate driver(s) that offers overlap protection (interlock) to prevent outputs VOA and VOB from being high at the same time, such as the Skyworks Si823x series.
Recommended deadtimes guidelines.

<table>
<thead>
<tr>
<th>Device</th>
<th>Ciss</th>
<th>Single Rg</th>
<th>Total Switching Time</th>
<th>Deadtime</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP65H070G4PS</td>
<td>638pF</td>
<td>50 Ω</td>
<td>112.8ns</td>
<td>220ns</td>
<td>Estimated</td>
</tr>
<tr>
<td>TP65H050G4WS</td>
<td>1000pF</td>
<td>45 Ω</td>
<td>159.7ns</td>
<td>250ns</td>
<td>Estimated</td>
</tr>
<tr>
<td>TP65H035G4WS</td>
<td>1500pF</td>
<td>30 Ω</td>
<td>174ns</td>
<td>330ns</td>
<td>Dead time tested</td>
</tr>
<tr>
<td>TP65H015G5WS</td>
<td>5200pF</td>
<td>15 Ω</td>
<td>237.4ns</td>
<td>430ns</td>
<td>Dead time tested</td>
</tr>
</tbody>
</table>

- Place the RCDCL (required) as close as possible to the drain pin of the high-side GaN FET and ground it to the large ground plane.
- SMD mounting is recommended for all snubber components.
- A Gate resistor (Rg) is required for all devices.
- Gate ferrite beads (FB1) are required for all devices.
- If a smaller than recommended gate resistor is used, then a switching node RC snuber (RCSn) is recommended.
- The gate ferrite bead and gate resistor prevent oscillation and reduce excessive di/dt when the GaN device is used in a half-bridge topology.
- The RCSn slightly reduces light and medium load efficiency with the benefit of increased output power.
- The RCSn implementation in a half-bridge has the advantage of allowing a higher peak turn-off switching current due to the reduction of the di/dt seen by the freewheeling device as the main conducting device turns off.
2) Recommended External Components for Gate Drive Circuit (may vary with PCBA layout)

![Diagram](image)

Figure 5. Driving circuits: (a) Singles ended with dual Rg – only used for dv/dt EMI control (b) Single output driver with a single Rg, (c) single output driver with different turn-on and turn-off Rg

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Voltage Drive</td>
<td>5/15Ω</td>
<td>10/30Ω</td>
<td>50Ω to 150Ω</td>
<td>0Ω to 10Ω</td>
<td>200Ω-300Ω</td>
<td>65Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>2Ω</td>
<td>5Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>50Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>5Ω</td>
<td>10Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>10Ω</td>
<td>20Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>20Ω</td>
<td>40Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>30Ω</td>
<td>60Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>50Ω</td>
<td>100Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>70Ω</td>
<td>140Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>100Ω</td>
<td>200Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
<tr>
<td>Recommended Single Gate Resistor (Rg) - only used for dv/dt EMI control</td>
<td>150Ω</td>
<td>300Ω</td>
<td>5Ω to 10Ω</td>
<td>65Ω to 100Ω</td>
<td>65Ω to 100Ω</td>
<td>100Ω</td>
</tr>
</tbody>
</table>

Table 2. Recommended components for single ended and half-bridge circuits.

3) To Verify GaN FET Stable Operation

To verify adequate operational margin without oscillation, as a minimum observe the Vos waveforms at the turn-on and turn-off switching edges at the application’s maximum drain current. This may occur during start-up or at the application’s maximum load step. A double-pulse or multi-pulse test is highly recommended utilizing the actual layout, with current levels at or greater than 120 percent of the application’s anticipated peak current. Verify that the ringing on the Vos waveform at the transition edges is adequately damped. See design guide DG004: Multi-pulse Testing for GaN Layout Verification.

The driver circuits with different configurations of driver and gate resistor are shown in Figure 5. A proper gate resistor is effective to limit the switching di/dt and keep the switching stable. As described in part III, the di/dt limit only applies to the device acting as a free-wheeling diode (FWD), i.e. the turn-off switching speed of the active device should be controlled, and only large turn-off Rg should be chosen but turn-on Rg can be small to reduce the turn-on power loss (except for single ended or flyback topologies where turn on is more important to reduce EMI and di/dt is not an issue due to no device operating as a FWD). The separate turn-on and turn-off Rg can be achieved using a Schottky diode in series with a Rg(on) resistor paralleling with a Rg(off) resistor, as shown in Figure 5 (c). It should be noticed that the direction of diode is different from that in the gate driving circuit of Si MOSFET. The equivalent Rg(on) is Rg(on) + Rg(off)/(Rg(on)+Rg(off)), and turn-off Rg value is same with Rg(off). The equivalent Rg(on) will be used if a dual output driver IC is used. Although there is no di/dt limit for turn-on, a proper Rg(on) should be carefully selected.
• to avoid cross-talk issues in high-speed switching half bridge circuit using 3 pin TO-220 and TO-247 packaged devices.
• EMI issues for single ended topologies such as flyback.