

650V GaN FET PQFN

Preliminary Datasheet

Description

The TP65H300G4LSG 650V, 300mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

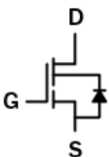
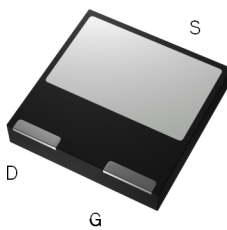
Related Literature

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0010](#): Paralleling GaN FETs

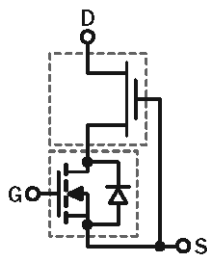
Product Series and Ordering Information

Part Number	Package	Package Configuration
TP65H300G4LSG	8x8mm PQFN	Source

**TP65H300G4LSG
PQFN
(top view)**



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)}$ production tested
- Robust design, defined by
 - Intrinsic lifetime tests
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter

Key Specifications	
V_{DS} (V) min	650
$V_{(TR)DSS}$ (V) max	720
$R_{DS(on)}$ (mΩ) max*	290
Q_{RR} (nC) typ	23
Q_G (nC) typ	9

* Dynamic $R_{DS(on)}$; see Figures 19 and 20

TP65H300G4LSG—Preliminary

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V	
$V_{(TR)DSS}$	Transient drain to source voltage ^a	720		
V_{GSS}	Gate to source voltage	± 18		
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	25	W	
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$ ^b	8	A	
	Continuous drain current @ $T_c=100^\circ\text{C}$ ^b	5	A	
I_{DM}	Pulsed drain current (pulse width: 10 μs)	30	A	
T_c	Operating temperature	Case	-55 to +150	$^\circ\text{C}$
T_J		Junction	-55 to +150	$^\circ\text{C}$
T_s	Storage temperature	-55 to +150	$^\circ\text{C}$	
T_{SOLD}	Soldering peak temperature ^c	260	$^\circ\text{C}$	

Notes:

- In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$
- For increased stability at high current operation, see Circuit Implementation on page 3
- For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Maximum	Unit
$R_{\theta JC}$	Junction-to-case	3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient ^e	50	$^\circ\text{C}/\text{W}$

Notes:

- Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness)

TP65H300G4LSG—Preliminary

Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{(BL)DSS}	Maximum drain-source voltage	650	—	—	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	1.6	2.1	2.6	V	V _{DS} =V _{GS} , I _D =0.5mA
R _{DS(on)eff}	Drain-source on-resistance ^a	—	240	290	mΩ	V _{GS} =8V, I _D =5A
		—	492	—		V _{GS} =8V, I _D =5A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current	—	1.2	10	μA	V _{DS} =650V, V _{GS} =0V
		—	5	—		V _{DS} =650V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V _{GS} =20V
	Gate-to-source reverse leakage current	—	—	-100		V _{GS} =-20V
C _{ISS}	Input capacitance	—	760	—	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	—	17	—		
C _{RSS}	Reverse transfer capacitance	—	TBD	—		
C _{O(er)}	Output capacitance, energy related ^b	—	25	—	pF	V _{GS} =0V, V _{DS} =0V to 400V
C _{O(tr)}	Output capacitance, time related ^c	—	48	—		
Q _G	Total gate charge	—	9	—	nC	V _{DS} =400V, V _{GS} =0V to 8V, I _D =5A
Q _{GS}	Gate-source charge	—	TBD	—		
Q _{GD}	Gate-drain charge	—	TBD	—		
Q _{OSS}	Output charge	—	19	—	nC	V _{GS} =0V, V _{DS} =0V to 400V
t _{D(on)}	Turn-on delay	—	TBD	—	ns	V _{DS} =400V, V _{GS} =0V to 12V, I _D =5
t _R	Rise time	—	TBD	—		
t _{D(off)}	Turn-off delay	—	TBD	—		
t _F	Fall time	—	TBD	—		

Notes:

- Dynamic R_{DS(on)} value; see Figures 19 and 20 for conditions
- Equivalent capacitance to give same stored energy from 0V to 400V
- Equivalent capacitance to give same charging time from 0V to 400V

TP65H300G4LSG—Preliminary

Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I _S	Reverse current	—	—	5	A	V _{GS} =0V, T _C =100 °C, ≤25% duty cycle
V _{SD}	Reverse voltage ^a	—	2.4	—	V	V _{GS} =0V, I _S =5A
		—	3.7	—		V _{GS} =0V, I _S =5A
t _{RR}	Reverse recovery time	—	TBD	—	ns	I _S =5A, V _{DD} =400V, di/dt=1000A/us
Q _{RR}	Reverse recovery charge	—	23	—	nC	

Notes:

- a. Includes dynamic R_{DS(on)} effect

TP65H300G4LSG—Preliminary

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003 : Printed Circuit Board Layout and Probing	

GaN Design Resources

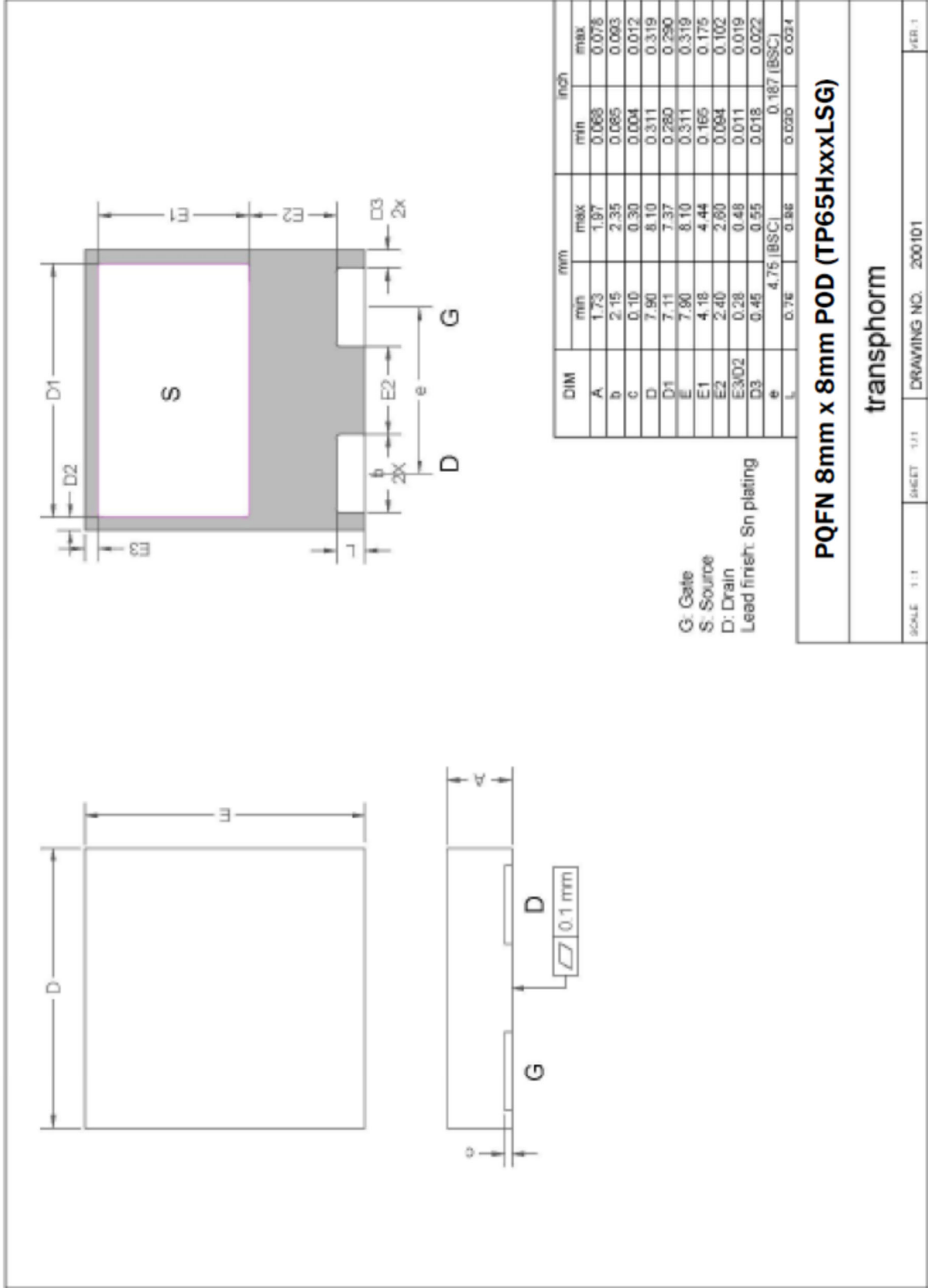
The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

TP65H300G4LSG—Preliminary

8x8 PQFN (LSG) Package

Mechanical



TP65H300G4LSG—Preliminary

Revision History

Version	Date	Change(s)
0	06/24/2019	Preliminary Datasheet