The Short-Circuit Current Limiter for GaN FETs: Delivering Higher Short-Circuit Capability Without Compromising Performance

Short-circuit capability of power switches is a critical feature for all power systems, particularly those more susceptible to experiencing short circuit events such as motor drives. These events caused by overload, shoot- through, current surge and/or external fault conditions (Figure 1) [1] require swift fault detection and safe turn off of power devices to prevent catastrophic failure.

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An adequate fault detection response time is approximately 2 µs [2], a time that dictates the desired Short-Circuit Withstanding Time (SCWT) rating of a power switch (i.e., the minimum time during which a device can withstand a short-circuit event, with both high voltage and high current applied between source and drain terminals.)
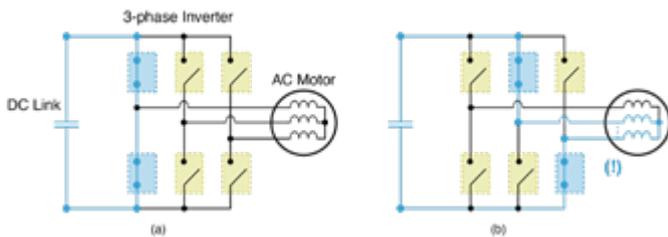

Figure 1: Power devices employed in a 3-phase motor drive scheme, showing two short-circuit scenarios: (a) shoot-through between high-side and low-side and (b) short-circuit across the inductive load.

To support continued adoption of high voltage GaN FETs, it's important to ensure a high SCWT. Though, given their inherent attributes, this can be difficult. GaN FETs, along with other wide bandgap devices, deliver much higher power density in smaller areas than conventional silicon devices. Consequently, when subjected to short-circuit conditions (simultaneous high voltage and high current surges and extreme instantaneous power dissipation), GaN devices may experience a steeper rise in temperature resulting in shorter SCWT than silicon-based counterparts.

Adequate Protection, Reduced Performance…
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The ability to achieve a SCWT ≥ 3 µs at 400 V with a 600 V GaN device has been demonstrated in research [3]. However, performance suffers as the reported normalized R_{on} of the device is greater than 20 $\Omega \cdot mm$ (> 9 $m\Omega \cdot cm^2$), rather high for market adoption.

Commercially available 600 V GaN devices haven't fared much better. When tested at 400 V, the SCWT of commercial devices with competitive specific R_{on} has been limited to < 0.5 µs [4] [5]. Increasing SCWT of GaN devices while maintaining a competitively low specific on-state resistance is therefore crucial to achieve short-circuit capability without performance compromise.

The Solution: Short-Circuit Current Limiter
Using a patented technology [6] [7] called the Short-Circuit Current Limiter (SCCL) (Figure 2), power dissipated during short-circuit events can be controlled—kept to a lower level—by reducing the short-circuit current flowing from drain to source with minimal degradation of the on-state resistance. In the two-chip normally-off GaN platform, lower short-circuit current and higher SCWT can be achieved by controlling either the saturation-current ($I_{d,sat}$) of the Si-FET or the saturation-current of the GaN-HEMT.
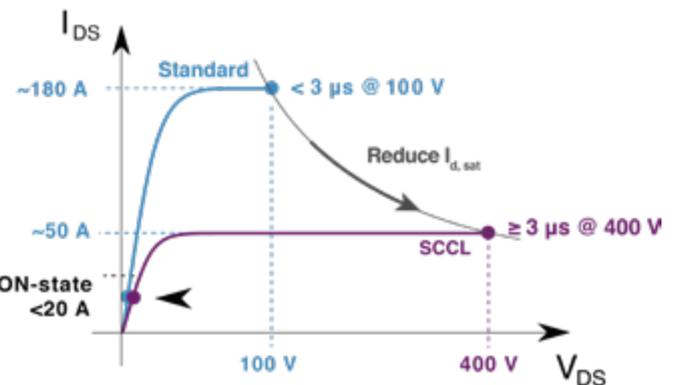

Figure 2: The patented Short-Circuit Current Limiter (SCCL) acts to reduce the drain-source saturation-current (I   ) to increase the SCWT of the device while preserving low on-state resistance.

For the purposes of analysis, the latter was performed: increasing SCWT by reducing the $I_{d,sat}$ of the GaN-HEMT.

The SCCL was implemented on Transphorm's core technology by removing segments of the 2DEG channel along the width of the GaN-HEMT by using a proprietary process. The top-view of a standard GaN-HEMT and a GaN-HEMT with SCCL are shown in Figures 3a and Fig. 3b, respectively. Longitudinal cross-sections of the SCCL device are shown in Figure 3c and Figure 3d. The section AA' is taken along current aperture path, where the 2DEG is uninterrupted from source to drain and electrons can flow in the on-state. In the aperture, the 2DEG properties (charge density and mobility) and the pinch-off voltage of the field-plate structure are the same as the standard device.

The section BB' is taken along current-blocking path, showing the lack of 2DEG under a limited portion of the field-plate structure. The proper design of the current-blocking segmentation (length, width and periodicity of the current block areas) ensures a good control of the saturation current while maintaining a competitively low on-resistance. Limited increase in R_{on} is possible because the R_{on} is mostly determined by the GaN-HEMT drain-access region (the equivalent of the "drift region" in a conventional power device), which is not affected by the SCCL blocking area. In fact, to control $I_{d,sat}$, it is sufficient to deploy the current block only in a small length along the entire source-drain spacing.
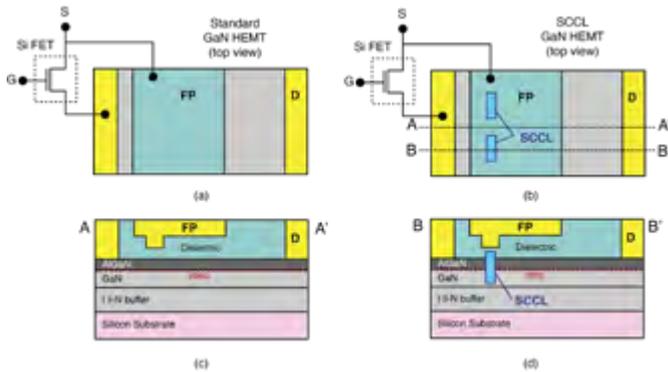

Figure 3: Top-view of two-chip normally-off GaN switch (a) without and (b) with the patented Short-Circuit Current Limiter (SCCL). The SCCL is implemented by removing segments of the 2DEG channel along the width of the GaN HEMT. Longitudinal cross-sections taken along paths featuring (c) the current aperture, and (d) the current block. Drawings are not to scale.

Experimental Results

A standard GaN device [8] was compared to a GaN device with SCCL. Both devices have the same chip-area, have the same 650 V rating, and have been packaged in 8x8 mm PQFN.

Figure 4 shows the room-temperature output characteristics: when the gate is fully on (Vgs = +12 V), the standard device has an average static R_{on} of 53 mΩ and a saturation current ($I_{d,sat}$) that exceeds 120 A, whereas the device with the SCCL has an average static R_{on} of 71 mΩ and a significantly lower $I_{d,sat}$ of 42 A. With the SCCL technology, we are able to achieve a 3x reduction in $I_{d,sat}$ with only a 0.35x increase in static on-resistance (Figure 5a).
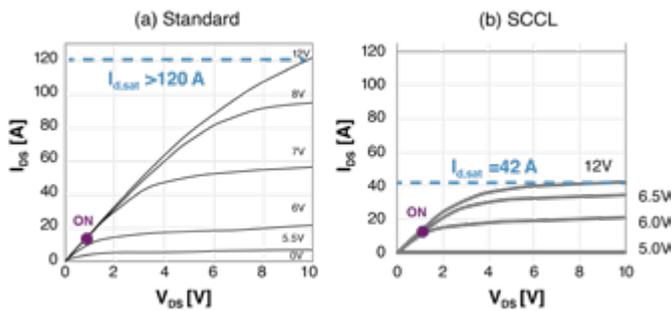

Figure 4: Room-temperature output curves of (a) standard 650-V GaN device and (b) 650-V GaN device with SCCL. When the gate is fully on (Vgs = +12 V), the standard device has a saturation current ($I_{d,sat}$) that exceeds 120 A, whereas the device with the SCCL has a significantly lower $I_{d,sat}$ of 42 A. A 3x reduction in $I_{d,sat}$ is achieved. with only a 0.35x increase in on-resistance.

It's worth noticing that, although the SCCL device has significantly lower $I_{d,sat}$ than the standard device, the SCCL $I_{d,sat}$ is still more than 2x higher than the maximum rated DC-current (20 A at room temperature). This is important to ensure not only good on-state operations, but also fast switching and fast discharge of the output capacitance (C_{oss}) during turn-on transients. Finally, the SCCL technology does not degrade the quality of the field-plate dielectric

isolation, as no increase in 650 V off-state leakage current has been observed with respect to the standard device (Figure 5b).
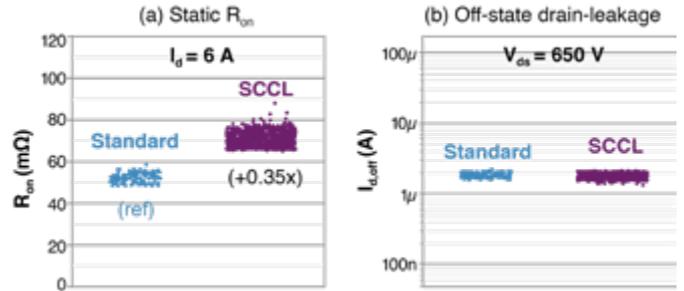

Figure 5: (a) Virgin static R_{on} acquired at room temperature with an on-state Id = 6 A. The SCCL device has a relatively small R_{on} penalty of +0.35x, as the current block is deployed only in a short section of the entire drain-source length. (b) Off-state drain leakage current acquired at V_{ds} = 650 V at room temperature. No increase in off-state leakage indicates that the SCCL technology does not degrade the quality of the field-plate dielectric isolation.
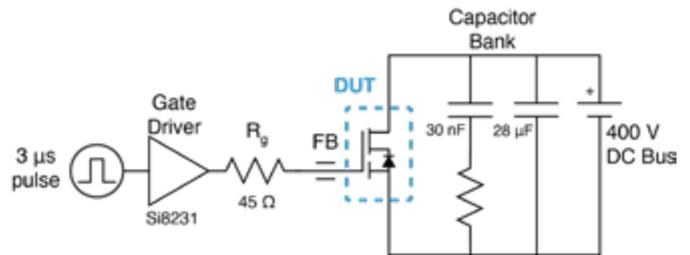

Figure 6: Schematic of the short-circuit test-board.
The board emulates a hard- switching fault, where the DUT is turned on directly onto a fault and experience the entire DC-bus voltage (400V) across its terminals.

To evaluate the SCWT improvement, devices were tested and compared with and without SCCL during short-circuit events under a worst-case scenario referred to as "hard-switch fault," where the DUT is turned on directly onto a fault and must withstand the full bus voltage for the entire duration of the short-circuit pulse. The short-circuit test-board is depicted in Figure 6. During the test, short-circuit events are emulated by fully turning on the gate for 3 μs. The DC-bus is increased step-by-step from 50 V to 400 V with 50 V increments. At each step, one short-circuit pulse was applied and the associated short-circuit waveforms were recorded. The tests reported in this work have been carried out at room temperature.

Results are shown in Figure 7. The standard device shows a short-circuit current of 180 A and fails after 3 μs at a DC-bus voltage of only 100 V, whereas the SCCL device has a much lower short-circuit current (50 A) and survives a 3-μs pulse at a voltage of 400 V. This remarkable increase in short-circuit robustness (of more than 4x) demonstrates the proof-of-concept and the successful implementation of the SCCL design.
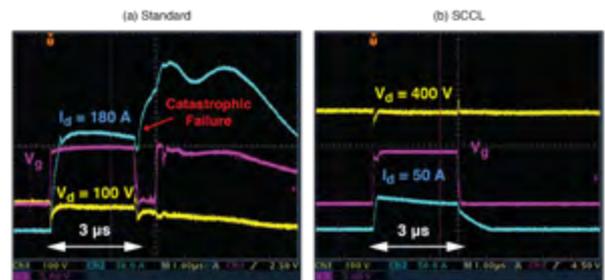

Figure 7: 3-μs short-circuit pulses acquired at room-temperature on (a) a standard GaN device and (b) a GaN device with SCCL. The standard device shows a short-circuit current of 180 A and fails at a DC-bus voltage of 100 V, whereas the SCCL has a much lower short-circuit current (50 A) and survives a 3-μs pulse at 400 V.

To ensure that SCCL devices can operate in actual real-world switching applications with high performance and high reliability, DC and short-circuit tests as well as dynamic R_{on} tests, inductive switching tests and High-Temperature Reverse Bias (HTRB) stress tests were carried out.

Dynamic R_{on} tests carried out with a DC-bus of 480 V and an on-state pulse-width of 2 μs show that the relative increase between dynamic and static R_{on} is approximately +18%. This is similar to the relative increase between dynamic and static R_{on} in standard devices and indicates that the SCCL blocking region does not exacerbate charge-trapping.

The inductive switching test carried out with a DC-bus of 400 V and a load current of 15 A (Figure 8) shows that, during both turn-on and turn-off, the pair of SCCL devices have similar dv/dt than the standard devices (≥35 V/ns with Rg = 50 Ω, Figure 9), indicating that the low $I_{d,sat}$ of the SCCL does not hamper the charging and discharging of the output capacitance (C_{oss}).
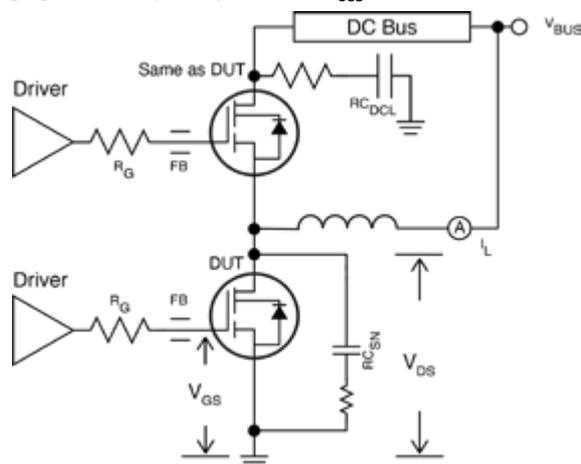

Figure 8: Schematics for the inductive switching test-board.

During HTRB tests, 80 parts were submitted to reverse-bias stress at 150°C and 520 V for 1000 hours. After both 250 hours and 1,000 hours, no fuse failure, no leakage increase, and a relatively small parametric R_{on} degradation (~5%) were observed. See Figure 10. The small parametric R_{on} degradation is similar to what was observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms. This is a promising result towards the prospective JEDEC and automotive qualifications of SCCL technology.

Conclusion

The SCCL proves to be a high performance, high reliability solution that improves the SCWT of GaN power devices to 3 μs at 400 V with
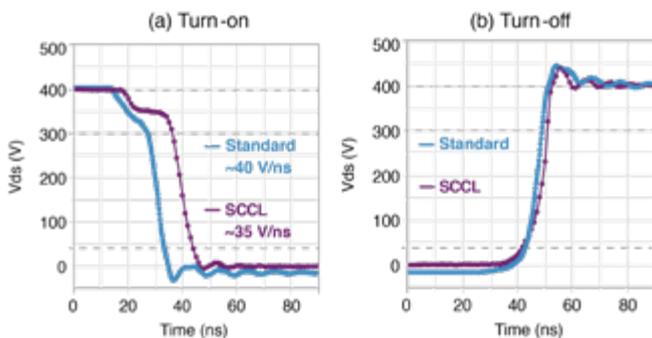

Figure 9: (a) Turn-on and (b) turn-off transients acquired with an inductive load current of ~15 A for both the standard device and the SCCL device. The SCCL device has similar dv/dt than the standard device, indicating that the low $I_{d,sat}$ of the SCCL does not hamper the charging and discharging of the output capacitance (C_{oss}).
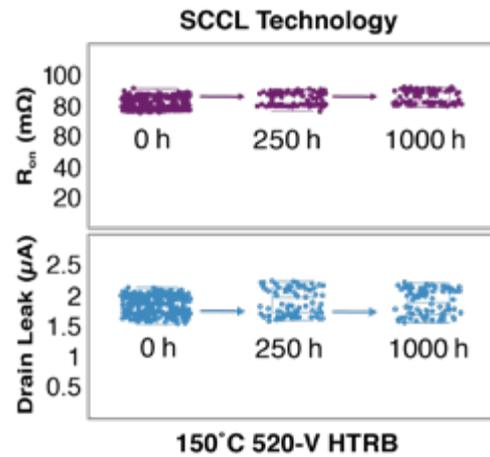

Figure 10: R_{on} and drain leakage measured before and after 1000-h HTRB test carried out at 150°C and 520 V on SCCL GaN devices (80 parts). After both 250 and 1000 hours, we observed no fuse failure, no leakage increase, and a relatively small parametric R_{on} degradation (~5%). The small parametric R_{on} degradation is similar to what observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms.

a limited increase in on-resistance. The SCCL reduces the short-circuit current by more than 3x and improves short-circuit robustness by more than 4x. As of today, the penalty in on-resistance is limited to 0.35x. Further reduction of the R_{on} penalty can be achieved by continuous optimization of the SCCL design. From an initial characterization campaign including dynamic R_{on} tests, inductive switching tests, and 100-h HTRB, the SCCL technology has demonstrated to have switching performance and reliability similar to standard Transphorm technology.

The SCCL technology can be applied to the entire portfolio of GaN products to serve a broad range of motor drive applications. Thanks to extended SCWT, the SCCL technology will allow the industry to adopt conventional short-circuit protection schemes, with sufficient immunity to noise and switching transients.

References
1. R. S . Chokhawala, J. Catt, L. Kiraly, "A Discussion on IGBT Short-circuit Behavior and Fault Protection Schemes," IEEE Trans. Industry Applications, vol. 31, p. 256, 1995. DOI: 10.1109/28.370271.
2. Mitsubishi Electric Corporation, "1200V Large DIPIPM Ver.6 Series Application Note PSS**SA2FT," 2020.
3. T. Nagahisa, H. Ichijoh, T. Suzuki, A. Yudin, A. O. Adan, M. Kubo, "Robust 600V GaN high electron mobility transistor technology on GaN- on-Si with 400V, 5 μs load-short-circuit withstand capability," Jpn. J. Appl. Phys., vol. 55, p. 04EG01, 2016.
4. M. Fernandez, X. Perpina, J. Roig-Guitart, M. Vellvehi, F. Bauwens, M. Tack, X. Jorda, "Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs," IEEE Trans. on Industrial Electronics, vol. 64, no. 11, p. 9012, 2017.
5. P. Williford, F. Wang, S. Bala, J. Xu, "Short Circuit Study of 600 V GaN GITs," in 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, USA, 2019.
6. Y. Wu, U. Mishra and S. Chowdhury, "SEMCONDUCTOR ELECTRONIC COMPONENTS WITH INTEGRATED CURRENT LIMITER". U.S. Patent 9443849, 13 Sep 2016.
7. U. Mishra, S. Chowdhury and I. Ben-Yaacov, "SEMICONDUCTOR DEVICES WITH INTEGRATED HOLE COLLECTORS". U.S. Patent 9184275, 10 Nov 2015.
8. Transphorm Inc., "TP65H070 Series," [Online]. Available: https://www.transphormusa.com/en/product/tp65h070lsg/.